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MonolithIC 3D – General

By MonolithIC 3D Inc.

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About the authors of the e-book

Zvi Or-Bach
President and CEO

Zvi Or-Bach is the founder of MonolithIC 3D™ Inc., a Finalist of the “Best of Semicon West 2011” for its monolithic 3D-IC breakthrough. Or-Bach was also a finalist of the EE Times 2011 and 2012 Innovator of the Year Award for his pioneering work on the monolithic 3D-IC.

Or-Bach has a history of innovative development in fast-turn ASICs for over 20 years. His vision led to the invention of the first Structured ASIC architecture, the first single via programmable array, and the first laser-based system for one-day Gate Array customization. In 2005, Or-Bach won the EETimes Innovator of the Year Award and was selected by EE Times to be part of the **"Disruptors" --"The People, Products and Technologies That Are Changing The Way We Live, Work and Play"**.

Prior to MonolithIC 3D, Or-Bach founded eASIC in 1999 and served as the company's CEO for six years. eASIC was funded by leading investors Vinod Khosla and KPCB in three successive rounds. Under Or-Bach's leadership, eASIC won the prestigious **EE Times' 2005 ACE Award for Ultimate Product of the year** in the Logic and Programmable Logic category.

Earlier, Or-Bach founded Chip Express in 1989 (recently acquired by Gigoptix) and served as the company's President and CEO for almost 10 years, bringing the company to $40M revenue, and to an industry recognition for three consecutive years as a high-tech Fast 50 Company that served over 1000 ASIC designs, including many one-day prototypes and one-week production delivery.

Even before his entrepreneurial ventures in ASIC technology, Or-Bach held engineering management positions at Elbit Computers, Ltd., Israel (subsidiary of Elron) and Honeywell (Lexington, Massachusetts). Zvi Or-Bach received his B.Sc. degree (1975) cum laude in Electrical Engineering from the Technion - Israel Institute of Technology, and M.Sc. (1979) with distinction in Computer Science, from the Weizmann Institute,

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Israel. He holds over 100 issued or pending patents, primarily in the field of 3D integrated circuits and semi-custom chip architectures. He is the Chairman of the Board for Zeno Semiconductors, Bioaxial and VisuMenu. Or-Bach is passionate about the semiconductor industry, and has participated in **initiatives to improve immigration and education policies** to benefit the same.

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Brian Cronquist
Vice President, Technology & IP

Brian Cronquist has over 31 years of semiconductor industry experience, most recently as Sr. Dir. Technology Development & Foundry at non-volatile FPGA provider Actel. He has global experience on “both sides of the silicon wafer table”: starting and building Chartered Semiconductor (Singapore) technology and customers as a captive then pure foundry, and non-volatile (antifuse and flash) FPGA technology at Actel as a fabless partner and customer to over 7 foundries and IDMs. He also led startup wafer fab engineering teams at Sierra Semiconductor, now PMC-Sierra, and developed new process technology at AMI and Synertek/Honeywell.

Mr. Cronquist has a diverse technical interest which includes developing ultra-thin thermal oxide and pre-cleaning technology (first to develop and implement HF-last), plasma etching of metals and oxides, database scaling techniques, process simulation & integration, novel ion implant techniques, first CMOS MOSFETs built with laser (CW) annealing, minimizing process induced damage PID) from plasma etching and ion implantation, time-to-market new product and process introduction (NPI), and customer engineering & program management.

While at Actel, he was also Principal Investigator of over $24M of government funded technology programs developing radiation hardened (RH) versions of both anti-fuse and flash based product families in commercial and RH foundries. He has published over 85 technical papers in the fields of semiconductor microelectronic radiation effects and hardening, as well as new logic, antifuse & flash processes, devices, and reliability. Mr. Cronquist graduated cum laude (Chemistry Medal) in Chemistry from Santa Clara University in 1979. Currently, he is a visiting researcher at the Rice University Chemistry Department and an Industry Affiliate Partner at the Stanford University Nanofabrication Facility.

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Ze'ev Wurman

Chief Software Architect

Wurman has over 30 years of experience in developing algorithms, CAD software, and hardware and software architectures. Before MonolithIC 3D Inc., he led the software development groups in DynaChip, an FPGA startup later acquired by Xilinx, and eASIC, a programmable logic company. Prior to that Wurman was the architect for hardware simulation accelerator at Amdahl, the largest and fastest hardware accelerator at the time. He designed and managed CAD software for Silvar-Lisco, and spent three years with IBM Research in Haifa, Israel, working on algorithms for design verification, databases, and cryptography. Between 2007 and 2009 Wurman served as senior policy adviser in the office of Planning, Evaluation, and Policy Development, in the U.S. Department of Education.

Wurman holds B.Sc. and M.Sc. degrees in Electrical Engineering from Technion, Israel Institute of Technology, in Haifa, Israel. He has published technical papers in professional and trade journals and holds seven patents.

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Israel Beinglass, Ph.D.
CTO Device Integration

Dr. Israel Beinglass has over 25 years of diversified experience in the semiconductor and semiconductor equipment industries. From 1989 through 2006 he was a senior technologist and business executive at Applied Materials (NASDAQ:AMAT), the global leader in semiconductor equipment, where he served in a variety of executive roles. He was General Manager of the High Temperature Films Group, Managing Director and Chief Technology Officer (CTO) for the Front End Equipment Group, and later CTO of Applied Global Services Group. He also served as the Chief Marketing Officer (CMO) of the CMP division and CTO for the Thin Films Group (TFG). Dr. Beinglass was involved in numerous successful acquisitions and was a member of Applied Materials Strategy and Marketing councils.

Dr. Beinglass is the industry pioneer of selective deposition; he is the co-inventor of the selective tungsten deposition process and an earlier developer of selective Epi deposition. He also was instrumental in developing the industry's first single-chamber polysilicon deposition system and an integrated, multi-chamber Policide system.

Before joining Applied Materials, Dr. Beinglass worked at Intel Corporation (NASDAQ:INTC) and IMP (NASDAQ:IMPX) in various positions, including process development manager and engineering manager of fab operations. While working at Intel he was the inventor of the selective tungsten deposition process. He was a co-recipient of the Beatrice Winner Award for Editorial Excellence at the Intl. Solid State Circuits Conference in 1982. He serves as a board member at Noise Free Wireless and Spectros and used to serve as a board member at Silicon Genesis between 1998 and 2001.

Dr. Beinglass holds a Ph.D. in Materials Science from the Hebrew University of Jerusalem; he completed post-doctoral research at UCSF and is the holder of 30 US patents (288 citations) as well as several pending patents.

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Deepak Sekar, Ph.D.

Former Chief Scientist

Dr. Deepak Sekar received a B. Tech from the Indian Institute of Technology (Madras) in 2003 and a PhD from the Georgia Institute of Technology in 2008. He worked at SanDisk Corporation between 2006 and 2010, and conducted research on non-volatile memory. He joined MonolithIC 3D™ Inc. in early-2010 as a Principal Engineer, in 2011 as Chief Scientist of the company and left the company in March 2012.

For the past 8 years, Dr. Sekar's research has focused on 3D Integrated Circuits. His PhD research involved doing some of the first experimental work on microchannel cooled 3D stacked chips. He also developed a CAD tool called IntSim that simulates 2D and 3D stacked systems. At SanDisk, Dr. Sekar worked in the area of 3D crosspoint memory and developed rewritable memory devices, selector diodes and array architectures.

Dr. Sekar is the author of a book, an invited book chapter, 15 publications and 55 issued or pending patents, predominantly in the field of 3D integration. Awards he has received include a Best Student Paper Award at the Intl. Interconnect Technology Conference (2008), a Best Paper Award at the IETE Technical Review (2009), an Intel PhD Fellowship (2006-2008), a Motorola Electronic Packaging Fellowship Award at the Electronic Components and Technology Conference (2008), two Inventor Recognition Awards from the Semiconductor Research Corporation (2006, 2009) and the National Talent Scholarship from the Government of India (1997-2003). He serves as a Program Committee Co-Chair at the International Interconnect Technology Conference and as an Advisory Board Member for 3D InCites.

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Part 1: Monolithic 3D - General

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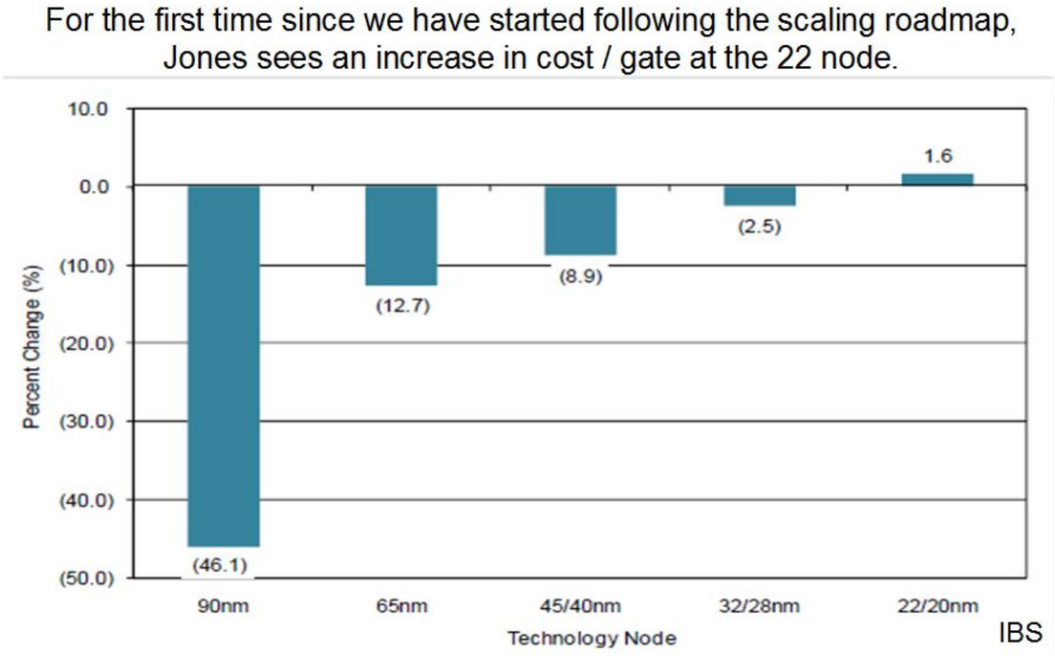
Chapter 1 - Is the Cost Reduction Associated with Scaling Over?

by Zvi Or-Bach, the President and CEO of MonolithIC 3D Inc.

"Yes, unless we Augment Dimensional Scaling with monolithic 3D-IC Scaling"

The last 50 years of the semiconductor industry have been all about the manifestation of Moore's Law in dimensional scaling of Integrated Circuits (ICs). As consumers of electronic devices we all love to see with every new product cycle better products at a lower cost. But now storm clouds are forming, as was recently publicly expressed "Nvidia deeply unhappy with TSMC, claims 20nm essentially worthless".

Clearly dimensional scaling is no longer associated with lower average cost per transistor. The chart below, published by IBS about a year ago, shows the diminishing benefit of cost reduction from dimensional scaling. In fact, the chart indicates that the 20nm node might be associated with higher cost than the previous node.



The following Nvidia chart provides the first order explanation. The cost reduction of dimensional scaling resulted from doubling the number of transistors per wafer. But if

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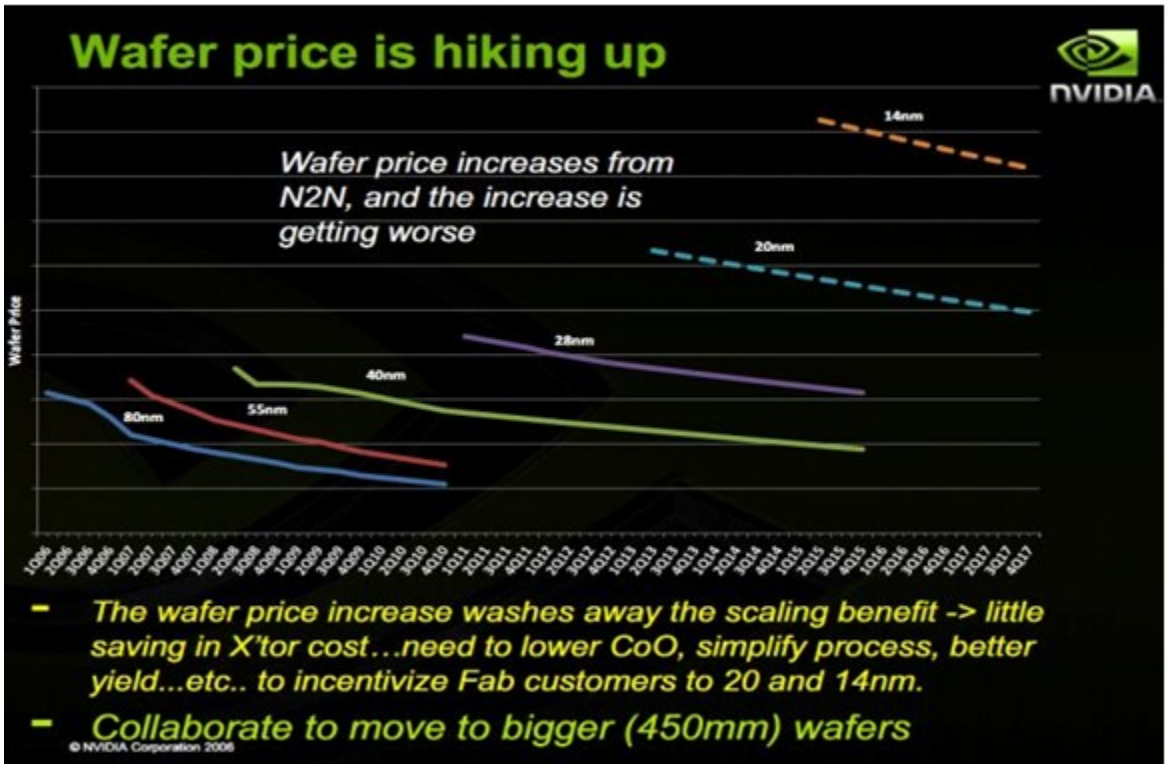
the wafer cost of the new technology node increases by too much then it neutralizes that cost reduction. The Nvidia chart shows the wafer cost of recent nodes over time. In the past (...80nm, 55nm, 40nm) the incremental wafer cost increases were small and rapid depreciation of those costs resulted in almost constant average wafer price. Recent nodes (28nm, 20nm, 14nm,...), however, signal a new reality.



The following busy slide of IBM summarizes it clearly: "Net: neither per wafer nor per gate showing historical cost reduction trends"

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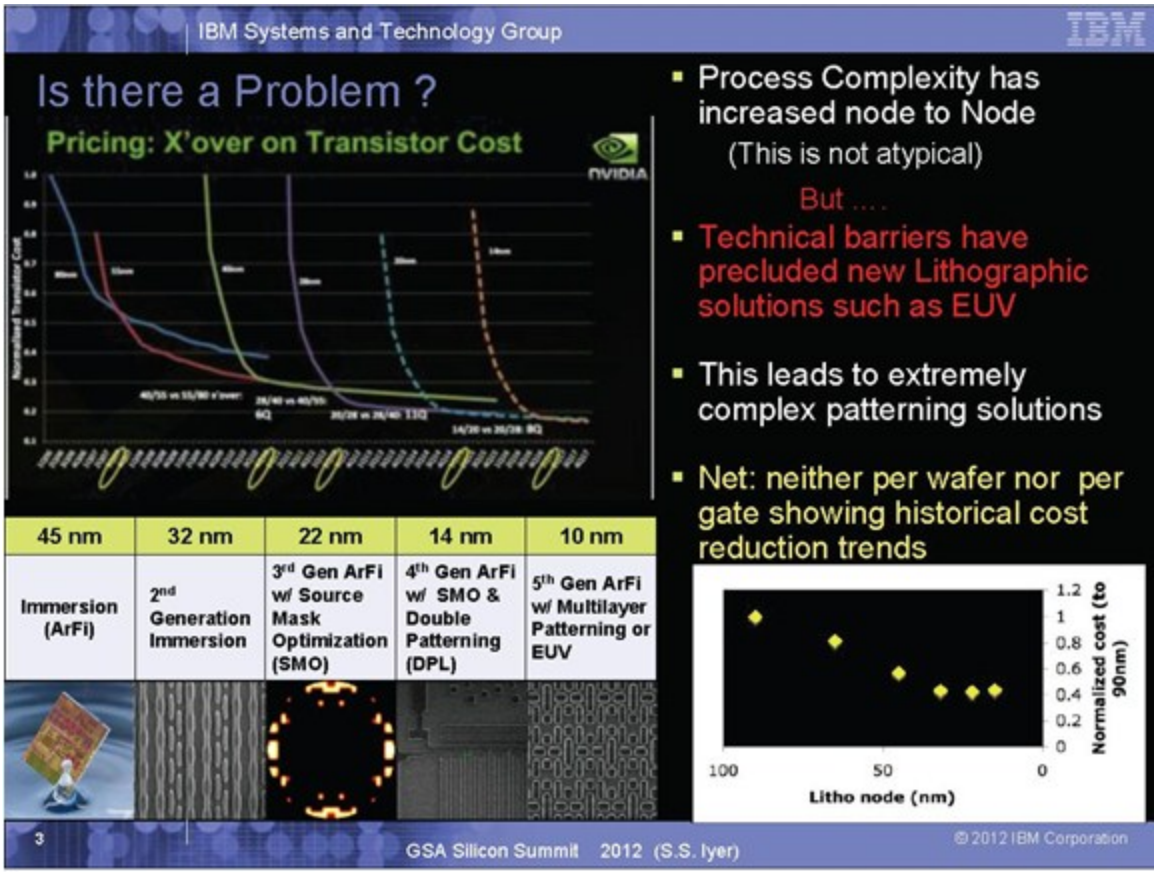
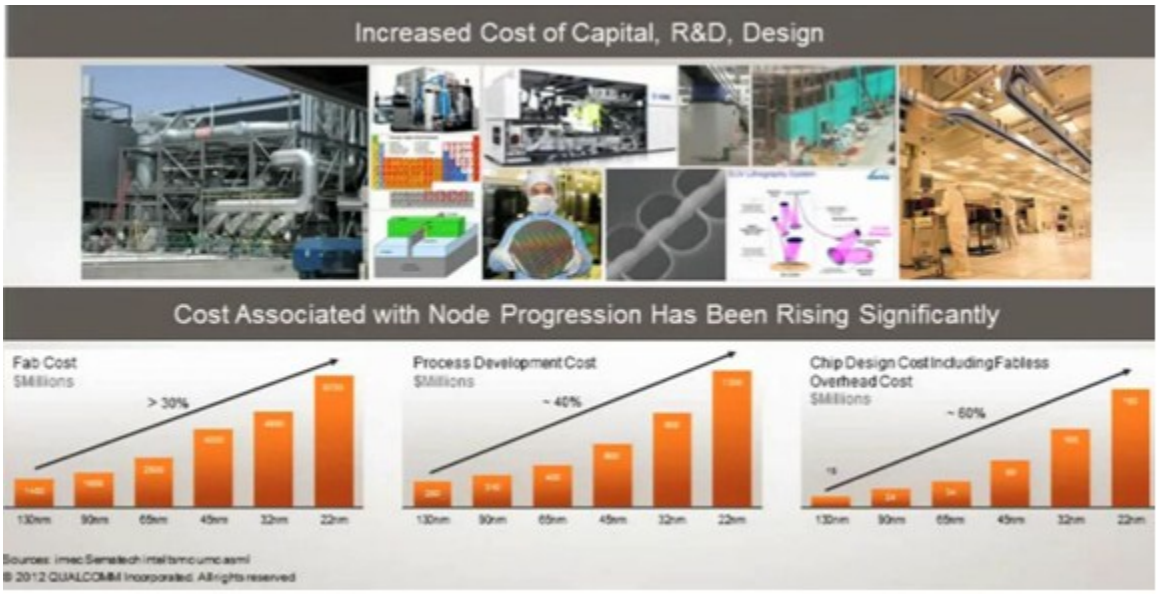
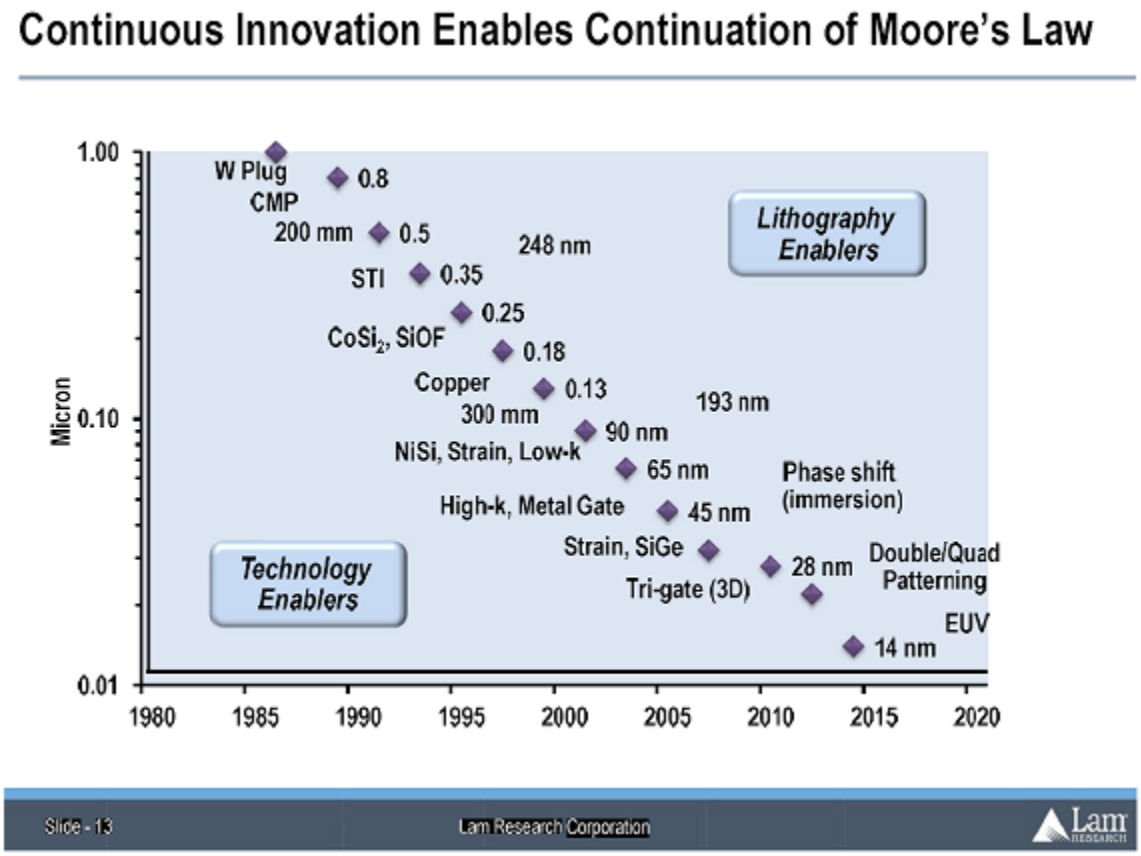


The number one driver to the increase of wafer cost is the increase in the equipment cost required for processing the next technology node. The following chart presents the increase in costs of capital, process R&D, and design.



The sharp increase of costs associated with scaling is a new phenomenon. There were always costs to move from one node to the next, but they were about constant or incrementally small.

The following slide presents the innovations that enable dimensional scaling. Clearly, for many nodes we were able to use the same lithography tools. But once dimensional scaling reached the limit of light wavelength the lithography tool became critical and dominant. About for every node the lithography became a major challenge that required newer equipment and substantial process R&D. Moreover, in the recent lithography nodes the transistor itself required significant innovation at every node (high-k, Metal Gate, Strain, SiGe, Tri-gate,...) and it is clear that future scaled nodes will require even more of those innovations and their associated costs.



An important part of these costs is the escalating cost of the capital equipment for the next node fabrication lines. The following figure present the cost dynamic for the lithography equipment. Note the logarithmic scale of the cost axis.

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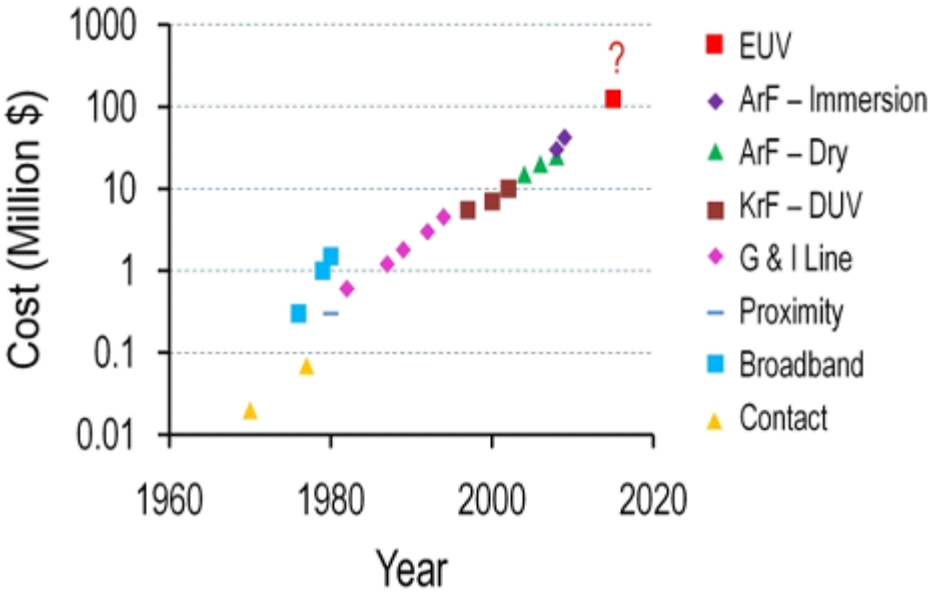

Lithography tools grew from less than 10% of wafer fab equipment (WFE) spending to over 25% and accordingly lithography now represents about 50 % of the wafer cost.

An interesting implication of growing domination of lithography in semiconductor processing is the fact that the ASML, which is the lead vendor of lithography tool, recently passed Applied Material's (the leader of all other tools) market cap. Following is the chart of the stock price of ASML (in red) vs. Applied Material (AMAT).

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The clear conclusion of all of this is that future dimensional scaling is not about to change these trends. Accordingly, as stated in the IBM slide above: "Net: neither per wafer nor per gate showing historical cost reduction trends." Unless ...

Unless we change the way we do scaling (remember Einstein's famous quote). Moore's Law is about doubling the number of transistors in a semiconductor device. At that time dimensional scaling was one of the three trends Moore described that would enable the observed and predicted exponential increase of device integration. It would seem that it is about time to look on another one of those - increasing the die size. If we do it by using the 3rd dimension – monolithic 3D-IC – we can achieve both higher integration and cost reduction!

It is not that we should stop scaling down, it just that if we augment it with scaling up we can introduce the required changes that can achieve the continuation of the cost reduction trend. Clearly almost all of the increases of wafer costs are related to the pace of dimensional scaling. If those costs could be spread over four years instead of two then the increase in wafer cost would be only about half of what it is now.

It might not be so clear, however, why monolithic 3D should reduce wafer cost. Shouldn't the cost of the double die size spread over two layers be at least double …?

Monolithic 3D IC would reduce wafer cost because of the following elements:

1. Reduced Die Size - It has been shown in many research studies that each folding into 3D has the potential to reduce the total required silicon area by 50% due to the reduced re-buffering and reduced sizing of the buffers.

2. Depreciation - Scaling up enables the use of the same fab and process R&D for few additional years with the associated improvement in deprecation costs and improved manufacturing efficiencies and yield.

3. Heterogeneous Integration - Scaling up would enable heterogeneous integration. This will open up the third trend of Moore- improved circuit design. As each strata of 3D IC could be processed in a different flow, cost and power could be saved by using a different process flow for logic, memory and I/O.

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