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Nanoelectronic Design Based on a CNT Nano-Architecture

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Abstract — Carbon nanotubes (CNTs) and carbon nanotube field effect transistors (CNFETs) have demonstrated extraordinary properties and are widely expected to be the building blocks of next generation VLSI circuits. This chapter presents (1) the first purely CNT and CNFET based nano-architecture, (2) an adaptive configuration methodology for nanoelectronic design based on the CNT nano-architecture, and (3) robust differential asynchronous circuits as a promising nano-circuit paradigm.

1. Introduction

Silicon based CMOS technology scaling has driven the semiconductor industry towards cost minimization and performance improvement in the past five decades, and is rapidly approaching its end (30). On the other hand, nanotechnology has achieved significant progress in recent years, fabricating a variety of nanometer scale devices, e.g., molecular diodes (44) and carbon nanotube field effect transistors (CNFETs) (46). This provides new opportunities for VLSI circuits to achieve continuing cost minimization and performance improvement in a post-silicon-based-CMOS-technology era.
However, we must overcome a number of significant challenges for practical nanoelectronic systems, including achieving some of the most critical nanoelectronic design metrics as follow.

1. Manufacturability. As minimum layout feature size becomes smaller than lithography light wavelength, traditional lithography based manufacturing process can no longer achieve satisfiable resolution, and leads to significant process variations. Resolution enhancement and other design for manufacturability techniques become less applicable as scaling continues. Alternatively, nanoelectronic systems are expected to be based on bottom-up self-assembly based manufacturing processes, e.g., molecular beam epitaxy (MBE). Such bottom-up self-assembly manufacturing processes provide regular structures, e.g., perfectly aligned carbon nanotubes (23). Consequently, nanoelectronic systems need to rely on reconfigurability to achieve functionality and reliability (51).
2. Reliability. Technology scaling has led to increasingly significant process and system runtime variations, including critical dimension variation, dopant fluctuation, electromagnetic emission, alpha particle radiation and cosmos ray strikes. Such variations cannot be avoided by manufacturing process improvement, and is inherent at nanometer

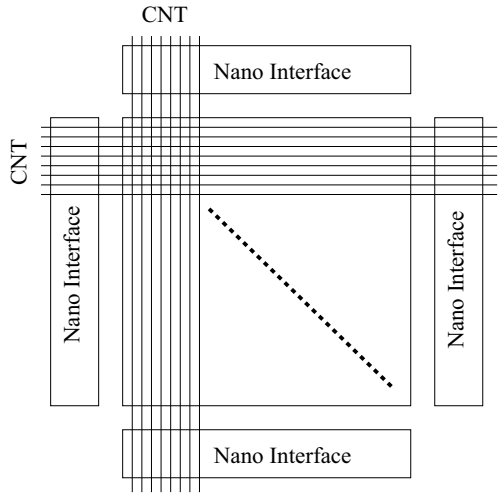

Fig. 1. The proposed CNT crossbar nano-architecture: layers of orthogonal carbon nanotubes form a dense array of RDG-CNFETs and programmable interconnects with voltage-controlled nano-addressing circuits on the boundaries.

scale due to the uncertainty principle of quantum physics. Robust design techniques, including redundant, adaptive, and resilient design techniques at multiple (architecture, circuit, layout) levels, are needed to achieve a reliable nanoelectronic system (5).

3. Performance. Nanoscale devices have achieved ultra-high performance in the absence of load, however, nanoelectronic system performance bottleneck lies in global interconnects. Rent's rule states that the maximum interconnect length scales with the circuit size in a power law (24), while signal propagation delay across unit length interconnect increases as technology scales (30). As a result, interconnect design will be critical to nanoelectronic system performance.
4. Power consumption. As technology scaling leads to increased device density and design performance, power consumption is also expected to be critical in nanoelectronic design.

This chapter presents several recent technical advancements towards manufacturable, reliable, high performance and low power nanoelectronic systems.

1. The first purely CNT and CNFET based nano-architecture, which is constructed by layers of orthogonal CNTs with via-forming and gate-forming molecules sandwiched in between, forming a dense array of reconfigurable double gate carbon nanotube field effect transistors (RDG-CNFETs) and programmable interconnects. Such a CNT array is addressed by novel voltage-controlled nano-addressing circuits on the boundaries, which do not require precise layout design and achieve yield in aggressive scaling and adaptivity to process variations. Simulation based on CNFET and molecular device compact models demonstrates superior logic density, reliability, performance and power consumption for nano-circuits implemented in this CNT crossbar based nano-architecture compared with the existing, e.g., molecular diode and MOSFET based nano-architectures.

2. A complete set of linear complexity methods for adaptive configuration of nanoelectronic systems based on a CNT crossbar based nano-architecture (Fig. 1) (26), including (1) adaptive nano-addressing, (2) RDG-CNFET gate matching, and (3) catastrophic defect mapping methods. Compared with the previous nano-architecture defect mapping and adaptive configuration proposals, these methods are complete, specific, deterministic, of low runtime complexity. These methods demonstrate the promising prospect of achieving nanoelectronic systems of correct functionality, performance, and reliability based on the CNT crossbar nano-architecture.
3. Robust Differential Asynchronous (RDA) circuits as a promising paradigm for reliable (noise immune and delay insensitive) high performance and low power nano-circuits based on the CNT crossbar nano-architecture. Theoretical analysis and SPICE simulation based on $22nm$ CMOS Predictive Technology Models show that RDA circuits achieve much enhanced reliability in logic correctness in the presence of a single bit soft error or common multiple bit soft errors, and timing correctness in the presence of parametric variations given the physical proximity of the circuit components.

The rest of this chapter is organized as follows. Section 2 reviews the existing nanoelectronic devices, nano-architectures and nano-addressing circuits. Section 3 presents the proposed CNT crossbar based nano-architecture including a novel RDG-CNFET device, a multi-layer CNT crossbar structure, and a voltage-controlled nano-addressing circuit. Section 4 presents adaptive configuration methods for nanoelectronic systems based on the CNT crossbar nano-architecture. Section 5 presents robust differential asynchronous circuits as a promising nano-circuit paradigm. Section 6 presents simulation results which evaluate the CNT crossbar nano-architecture and robust differential asynchronous nano-circuits. Section 7 concludes this paper with a list of nanotechnologies which enable and improve the proposed CNT crossbar based nano-architecture.

2. Background

2.1 Existing Nanoscale Devices

Carbon nanotube is one of the most promising candidates for interconnect technology at nanometer scale, due to its extraordinary properties in electrical current carrying capability, thermal conductivity, and mechanical strength. A carbon nanotube is a one-atom-thick graphene sheet rolled up in a cylinder of a nanometer-order diameter, which is semiconductive or metallic depending on its chirality. The cylinder form eliminates boundaries and boundary-induced scattering, yielding electron mean free path on the order of micrometers compared with few tens of nanometers in copper interconnects (32). This gives extraordinary current carrying capacity, achieving a current density on the order of $10^9 A/cm^2$ (56). However, large resistance exists at CNT-metal contacts, reducing the performance advantage of CNTs over copper interconnects (38).

Among various nanotechnology devices, carbon nanotube field effect transistors are the most promising candidates to replace the current CMOS field effect transistors as the building blocks of nanoelectronic systems. Three kinds of carbon nanotube based field effect transistors (CNFETs) have been manufactured: (1) A Schottky barrier based carbon nanotube field effect transistor (SB-CNFET) consists of a metal-nanotube-metal junction, and works on the principle of direct tunneling through the Schottky barrier formed by direct contact of metal and semiconducting nanotube. The barrier width is modulated by the gate voltage. This device has the most mature manufacturing technique up to today, while two problems limit its

future: (a) The metal-nanotube contact severely limits current. (b) The ambipolar conduction makes this devices cannot be applied to conventional circuit design methods. (2) A MOSFET-like CNFET is made by doping a continuous nanotube on both sides of the gate, thus forming the source/drain regions. This is a unipolar device of high on-current. (3) A band-to-band tunneling carbon nanotube field effect transistor (T-CNFET) is made by doping the source and the drain regions into p^+ and n^+ respectively. This device has low on-current and ultra low off current, making it potential for ultra low power applications. It also has the potential to achieve ultra fast signal switching with $< 60mV/decade$ subthreshold slope (46).
Molecular electronic devices are based on two families of molecules: the catenanes which consist of two or more interlocked rings, and the rotaxanes which consist of one or more rings encircling a dumbbell-shaped component. These molecules can be switched between states of different conductivities in a redox (reduction/oxidation) process by applying currents through them, providing reconfigurability for nanoscale devices (44).
A variety of reconfigurable nanoscale devices have been proposed. Resonant tunneling diodes based on redox active molecules are configurable on/off (44). Nanowire field effect transistors with redox active molecules at gates are of high/low conductance (17). Spin-RAM devices are of high/low conductivity based on the parallel/anti-parallel magnetization configuration of the device which is configured by the polarity of the source voltage (40). A double gate Schottky barrier CNFET is configurable to be a p-type FET, an n-type FET, or off, by the electrical potential of the back gate (25). A double gate field effect transistor with the back gate driven by a three state RTD memory cell is configurable to be a transistor or an interconnect, reducing reconfiguration cost of a gate array (4).

2.2 Existing Nanoelectronic Architectures

At least three categories of nanoelectronic architectures have been proposed. An early nanoelectronic architecture NanoFabrics was based on molecular resonant tunneling diodes (RTDs) and negative differential resistors (NDRs) (20). The insightful authors have observed that passive device (diode/resistor) based circuits lack signal gain to recover from signal attenuation, while combining with CMOS circuits compromises scaling advantages. They proposed latches based on negative differential resistors (NDRs), which, unfortunately, have become obsolete since the publication.
The majority of the existing nanoelectronic architectures are based on a hybrid nano-CMOS technology, with CMOS circuits complementing nano-circuits. In FPNI (50) (CMOL (54)), a nanowire crossbar is placed on top of CMOS logic gates (inverters). The nanowires provide programmable interconnects (and wired-OR logic), while the CMOS gates(inverters) provide logic implementation (signal inversion and gain). Such architectures achieve compromised scaling advantage in term of device density. DeHon (11; 13) proposed to combine programmable nanoscale diode logic arrays with fixed simple CMOS circuitry, e.g., of precharge and evaluation transistors as in domino logic for signal gain. Sequential elements need also to be implemented as CMOS circuits. However, the optimal size of a combinational logic block is typically small (e.g., of 30-50 gates), which results in significant CMOS circuitry overhead in such architectures. An exception is memory design, where CMOS technology provides peripheral circuitry such as address decoders and read sensors with moderate overhead, while nanotechnology provides scaling advantage in memory cells (17; 47; 63).
The third category of existing nanoelectronic architectures rely on DNA-guided self-assembly to form 2-D scuffles for nanotubes (42; 43) or 3-D DNA-rods (14). Such technologies target application in the far future.

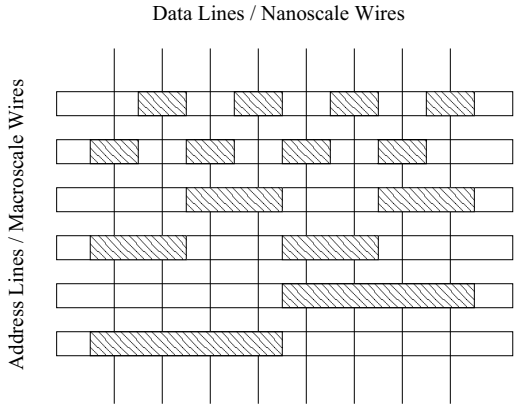

Fig. 2. Layout of undifferentiated nanoscale wires (data lines) addressed by microscale wires (address lines). Lithography defines high- and low-k dielectric regions, which gives field effect transistors and direct conduction, respectively.

2.3 Existing Nano-Addressing Circuits

A nano-addressing circuit selectively addresses a nanoscale wire in an array, and enables data communication between a nano-system and the outside world. The existing nano-addressing circuits are based on binary decoders, with an array of (microscale) address lines running across the (nanoscale) data lines, forming transistors at each crossing (e.g., Fig. 2). Each data line is selected by a unique binary address, given each data line has a unique gate configuration. However, such precise layout design is highly unlikely to achieve at a sublithographic nanometer scale (without significantly compromised yield).
In details, the existing nano-addressing circuits are in four categories as follow.

1. Randomized contact decoder (59) includes gold particles which are deposited at random as contacts between nanoscale and microscale wires. Testing and feedback provide a one-to-one mapping between a nanoscale wire and an address.
2. Undifferentiated nanoscale wires are addressable by microscale wires with (e.g., lithography defined) different gate configurations (which requires nanoscale wire spacing in the same order of lithography resolution) (22) (Fig. 2).
3. Alternatively, different gate configurations are realized in the nanoscale wires, by growing lightly-doped and heavily-doped carbon nanotubes of different length alternatively, while the microscale wires are undifferentiated. A microscale wire crossing a lightly-doped nanotube segment forms a gate, while a heavily-doped nanotube segment is always conductive for all possible signals in the microscale wire. In such a case, precise control of the lengths of the lightly- and heavily-doped nanotube segments would be critical (12; 21).
4. In radial addressing, multi-walled carbon nanotubes are grown with lightly- and heavily-doped shells, an etching process removes the heavily-doped outer shells at precise locations, and defines the gate configurations at each crossing of nanoscale and microscale wires (48).

Because process variations are inevitably significant at nanometer scale, these existing nano-addressing structures achieve limited yield, e.g., there is certain probability that two nanoscale wires have identical or similar gate configuration due to process variation. Furthermore, nanoscale wires are mostly partially selected, e.g., they may not achieve the ideal conductivity upon selected, due to process variations such as misalignment, dopant variation, etc.

2.4 Existing Nano-Architecture Defect-Mapping and Adaptive Configuration Methods

Existing nano-architecture defect mapping techniques are as follow. (1) On a Teramac reconfigurable computing platform, signals are propagated along each row or each column in a crossbar structure, a defect is located at the intersection of a defective row and a defective column, based on the assumption that a single defect is present (10). (2) In the NanoFabrics nano-architecture, the roughly estimated number of defects for a subset of computing resources are collected by counter or none-some-many circuits, a simple graph based algorithm or a Bayes' rule based probabilistic computation procedure gives defect occurrence probability estimates. E.g., highly likely defects are detected in the *probability assignment* phase, which accumulates defect probability in different test configurations, while less likely defects are located in the *defect location* phase, which incrementally clears certain spots as non-defects during test of different configurations (33). (3) A Build-In Self-Test (BIST) method in the NanoFabrics nano-architecture brings much increased complexity with limited applicability (in finding available defect-free neighboring nanoBlocks to implement test circuitry) (8; 58).
After a defect map is achieved presumably, logic circutis can be constructed avoiding or utilizing the defects. For example, a nanoPLA block can be synthesized in the presence of defective crosspoints (36), a CNT nano-circuit layout can be synthesized in the presence of misaligned and mispositioned CNTs (41), metallic CNTs (61), and CNTs of variational density (62).

2.5 Existing CNT Nano-Circuit Design

A very limited number of primitive combinational logic circuits have been fabricated based on CNFETs, including an inverter and two NOR gates in NMOS logic based on SB-CNFETs (3), and a five-inverter ring oscillator based on MOSFET-like CNFETs (9). While nano-circuits based on ambipolar SB-CNFETs need different topologies (3; 46; 53), nano-circuits based on unipolar MOSFET-like CNFETs can be identical to CMOS circuits (9).

3. CNT Crossbar based Nano-Architecture

As we have seen, most existing nanoelectronic architectures are based on diode/resistor logic and CMOS/nano-technologies (11; 13; 20; 50; 54; 63), which only achieve limited manufacturability, reliability, and performance. Carbon nanotubes (CNTs) and carbon nanotube field effect transistors (CNFETs) are the most promising candidates as the the building blocks of nanoelectronic systems due to their extraordinary properties. CNTs possess excellent electrical current carrying capability, thermal conductivity, and mechanical strength. CNFETs are potential to achieve high on-current, ultra-low off-current, and ultra-fast switching ($< 60mV/decade$ sub-threshold slope). CNT crossbar structure (Fig. 1) is one of the most promising candidates for nanoelectronic design platform. Recently, UIUC researchers have achieved fabrication of dense perfectly aligned CNT arrays (23). Such a CNT crossbar structure forms the basis of nanoscale memories (17; 47; 63).
However, no nanoelectronic architecture has been proposed which is solely based on CNTs and CNFETs. The reasons include lack of (1) a reconfigurable CNT based device which could provide functionality and reliability, (2) a self-assembly process which forms complex CNT

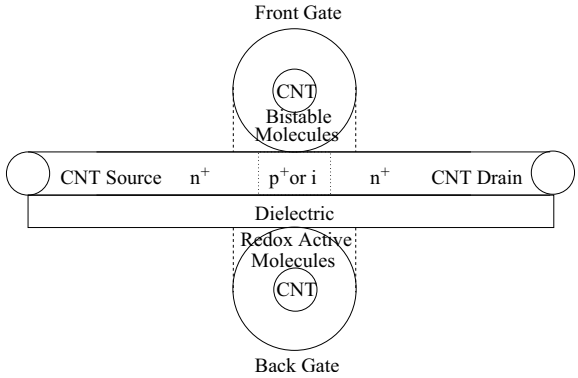

Fig. 3. A n-type MOSFET-like reconfigurable double gate carbon nanotube field effect transistor (RDG-CNFET).

structures, and (3) an achievable mechanism which precisely addresses an individual CNT in an array.

In this section, we investigate the first purely CNT and CNFET based nano-architecture, which is based on a novel RDG-CNFET device, includes a CNT crossbar structure on multiple layers, and a novel voltage-controlled nano-addressing circuit.

3.1 RDG-CNFET Device Structure

As the building block of a purely CNT and CNFET based nano-architecture, a reconfigurable double-gate CNFET (RDG-CNFET) is constructed by sandwiching electrically bistable molecules in a double gate CNFET. The double gate CNFET is constructed by three overlapping orthogonal carbon nanotubes. The top and the bottom carbon nanotubes form the front gate and the back gate, while doping the carbon nanotube in the middle layer forms the source and the drain of a n- or p-type MOSFET-like CNFET (46). Electrically bistable molecules are coated around the front gate and sandwiched between the front gate and the source/drain regions. Dielectric and redox active molecules are coated around the back gate and sandwiched between the back gate and the source/drain regions (Fig. 3).

The redox active molecules at the back gate are electrically reconfigurable to hold/release charge in a redox process, which controls the CNFET threshold voltage and conductance, or, turns the CNFET on or off. An example of such configuration is reported in (17), wherein a $\pm 10V$ voltage applied to cobalt phthalocyanine (CoPc) molecules triggers a redox process, and results in a NW-FET conductance change of nearly 10^4 times. Such reconfiguration of CoPc molecules is repeatable for more than 100 times.

The bistable molecules sandwiched between the front gate and the source/drain regions are electrically reconfigurable to be conductive or insular, making the device a via or a FET. An example of such electrically bistable molecules is reported in (44), wherein oxidative degradation reduces resonant tunneling current of the V-shaped amphiphilic [2]-rotaxane 5^{4+} molecules by nearly a factor of 100. Alternatively, the anti-fuse technologies in the existing reconfigurable architectures provide one-time configurability. For example, the QuickLogic ViaLink technology include a layer of amorphous silicon sandwiched between two layers of metal. A $10V$ programming voltage provides a resistance difference between $G\Omega$ and 80Ω (6).

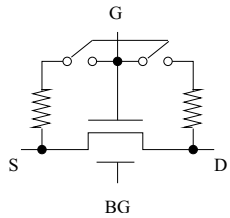

Fig. 4. Compact model of a n-type MOSFET-like reconfigurable double gate carbon nanotube field effect transistor (RDG-CNFET).

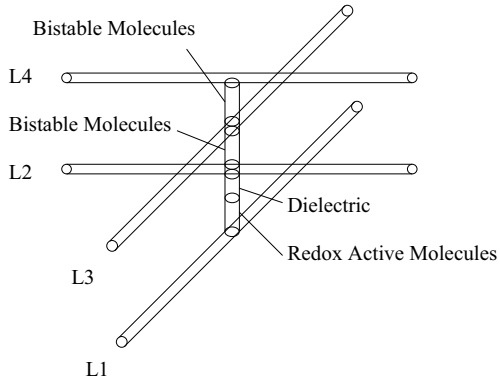

Fig. 5. Carbon nanotube (CNT) layers in the proposed nanoelectronic architecture.

3.2 RDG-CNFET Device Behavior

Such a RDG-CNFET device is described in a compact model as is shown in Fig. 4, and is reconfigurable to the following components, making it an ideal nanoelectronic architecture building block.

1. Via, when the front gate bistable molecules are configured to be conductive. The overlapping of the front gate and the source/drain regions form conductive contacts. As a result, the front gate, the source, and the drain are short circuited. The device is configured as a via between the carbon nanotubes on the top and in the middle.
2. Short, when the front gate bistable molecules are configured to be insular, and the back gate redox active molecules are configured to hold positive(negative) charge in a n-type(p-type) CNFET. The CNFET is on for any front gate voltage.
3. MOSFET-like CNFET, when the front gate bistable molecules are configured to be insular, and the back gate redox active molecules are configured to hold negative(positive) charge in a n-type(p-type) MOSFET-like CNFET. The CNFET threshold voltage is adjustable by the doping concentration in the channel (p or n doping for a n- or p-type CNFET), such that when the back gate redox active molecules are configured to hold negative(positive) charge in a n-type(p-type) MOSFET-like CNFET, the CNFET achieves both performance and leakage control.
4. Open, when the MOSFET-like CNFET is turned off. This is achieved at the architecture level as follows.

3.3 CNT Crossbar Structure

At a larger scale, a nanoelectronic architecture is constructed by growing layers of orthogonal carbon nanotubes, with via-forming (electrically bistable) and gate-forming (dielectric and redox active) molecules sandwiched at each crossing (Fig. 1). The carbon nanotubes are either (1) semiconductive CNTs which are doped to have low resistivity and are reconfigurable to opens by gate isolation, or (2) metallic CNTs which upon identification can be utilized as global interconnects if not avoided or removed (1; 64). The (1) via-forming (electrically bistable) and (2) gate-forming (dielectric and redox active) molecules can be first coated around a carbon nanotube (e.g., as in (17)), then undergo an etching process with the top layer of carbon nanotubes as masks (e.g., as in (49)). The remaining molecules are sandwiched between two orthogonal carbon nanotubes on adjacent layers. A top-down (e.g., lithography) process defines the areas for each type of molecules to assemble on each layer, as well as the p-wells and n-wells. P-type and n-type of MOSFET-like CNFETs are formed by (e.g., potassium or electrostatic (46)) doping of the carbon nanotubes selectively. E.g., a p-well or n-well of dimensions in the order of $22nm$ include about 10 rows of CNFETs.

Configuration of such a CNT crossbar based nanoelectronic architecture gives a nanoscale VLSI implementation including MOSFET-like CNFETs and interconnects with opens, shorts and vias (Fig. 6), which can be 2-D (compatible to traditional VLSI systems) or 3-D.

In a 2-D VLSI implementation, MOSFET-like CNFETs are formed on the bottom three layers of carbon nanotubes, with the first layer (L1) from bottom of carbon nanotubes provides the back gates, the second layer (L2) provides the source and the drain regions, and the third layer (L3) provides the front gates of the MOSFET-like CNFETs. Dielectric and redox active (back gate) molecules are sandwiched between the L1 and L2 layer carbon nanotubes, and electrically bistable (front gate) molecules are sandwiched between the L2 and L3 layer carbon nanotubes. A multi-layer reconfigurable interconnect structure with programmable vias and opens is achieved with via-forming and gate-forming molecules sandwiched between interconnects which are formed above the first (L1) layer (Fig. 5).

3-D VLSI circuits are under active research in recent years due to their potential of achieving reduced wirelength, reduced power consumption and improved performance. However, silicon based VLSI circuits are essentially 2-D, because MOSFETs are surface devices on the bulk of silicon, 3-D MOSFET circuits can only be achieved by bonding chips. It is therefore critical to achieve (1) bonding technology which provides acceptable mechanical strength, (2) via technology which provides low resistive interconnects between chips, and (3) heat dissipation in a multiple chip system for silicon based 3-D circuits. On the contrary, CNFET and CNFET based nano-architectures provide excellent platforms for 3-D VLSI circuits, because (1) CNTs and CNFETs are not confined to certain surface and can be manufactured in 3-D space, (2) CNTs possess excellent current carrying, mechanical and heat dissipation properties which are critical to 3-D VLSI circuits.

In a 3-D VLSI implementation, the RDG-CNFETs do not need to be confined on the bottom layers, with the upper layers dedicated to interconnects. Instead, transistors and interconnects are free to be located on each layer of carbon nanotubes. Gate forming (dielectric and redox active) molecules and via-forming (electrically bistable) molecules are distributed between adjacent CNT layers. Combination of the types of molecules surrounding a CNT segment gives three components.

1. Gate-forming molecules both on top and on bottom of a CNT segment give a device which is reconfigurable to either open or short,

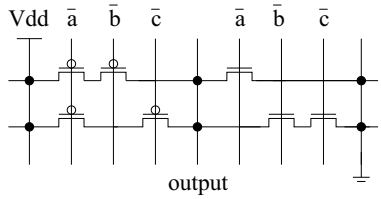

Fig. 6. An RDG-CNFET based Boolean logic $a(b+c)$ implementation.

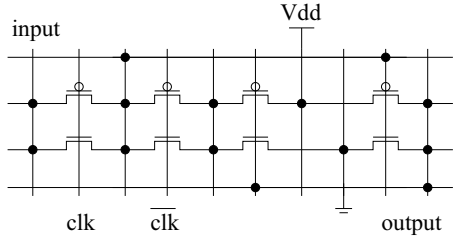

Fig. 7. An RDG-CNFET based latch implementation.

2. Gate-forming and via-forming molecules on top and on bottom of a CNT segment give the RDG-CNFET, which is reconfigurable to via, short, MOSFET-like CNFET, and open,
3. Via-forming molecules both on top and on bottom of a CNT segment give a device which is reconfigurable to be stacked via, simple via, or double gate FET.

We have the following observations.

Observation 1. *Via-forming (electrically bistable) molecules must be present between any two adjacent layers.*

Observation 2. *Gate-forming (redox active) molecules must be present next to each layer for gate isolation.*

Observation 3. *Gate-forming (redox active) and via-forming (electrically bistable) molecules need to be evenly distributed on each layer for performance.*

3.4 Circuit Paradigms and Analysis

This CNT crossbar based nano-architecture provides regularity and manufacturability for high logic density implementations of all CMOS logics, including the standard CMOS logic (e.g., in Fig. 6), domino logic, pass-transistor logic, etc., for combinational circuits, as well as latches (e.g., in Fig. 7), flip-flops, memory input address decoder and output sensing circuits. Such high logic density is achieved via direct connection of CNFETs through their source/drain regions (e.g., as in an latest Intel microprocessor implementation (15)), without going through additional (e.g., metal) interconnects. CNT-metal contacts are known to bring the most significant resistivity in CNT technology (38). Avoiding such CNT-metal contacts contributes to performance and reliability improvements. Furthermore, reduced interconnect length also leads to reduced interconnect capacitance, and improved circuit performance.
This CNT crossbar based nano-architecture also provides a high reconfigurability by allowing an arbitrary ratio of logic gates and interconnect switches (a RDG-CNFET device can be

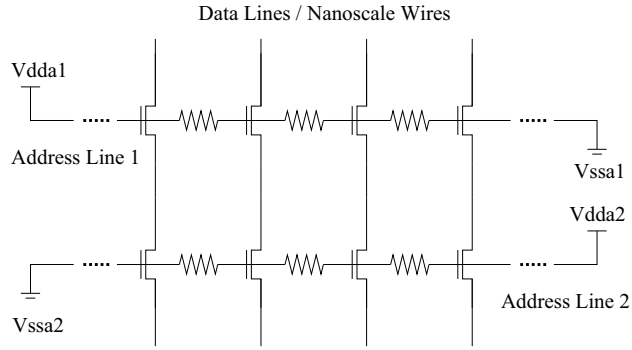

Fig. 8. Schematic of the proposed voltage-controlled nano-addressing circuit.

configured as either a logic gate or an interconnect switch). A pre-determined ratio of logic devices and interconnect switches (e.g., in standard cell designs and FPGA architectures where cells and routing channels are separated) constrains design optimization and may lead to inefficient device or interconnect utilization. Allowing an arbitrary ratio of logic gates and interconnect switches (e.g., as in sea-of-gate designs) provides increased degree of freedom for design optimization (4).

The CNT crossbar based nano-architecture is also the first to include multiple routing layers. Multiple routing layers (as in the current technologies) are necessary for VLSI designs, as Rent's rule suggests that the I/O number of a circuit module follows a power law with the gate number in the module (24). A small routing layer number could lead to infeasible physical design or significant interconnect detouring, resulting in degraded performance and device utilization.

3.5 Voltage Controlled Nano-Addressing Structure

The final piece of the CNT crossbar nanoelectronic architecture is the nano-addressing circuits on the boundary of the carbon nanotube crossbar structure.

Designing a nano-addressing circuit is a challenging task, because (1) the nanoscale layout cannot be manufactured precisely unless it is of a regular structure, and (2) the nano-addressing circuit cannot be based on reconfigurability since it provides reconfigurability to the rest of the nanoelectronic system.

A novel voltage-controlled nano-addressing circuit (Fig. 8) is constructed by running two address lines (of either microscale or nanoscale wires) on top of the data lines (of nanoscale wires in an array which are to be addressed). The address lines and the data lines are orthogonal. At each crossing of an address line and a data line, a field effect transistor is formed by doping the data line into the source and the drain regions while the address line provides the gate of the transistor, with a thin layer of dielectric sandwiched between the gate and the transistor channel. Such field effect transistors have been successfully fabricated based on either nanowires or carbon nanotubes (17; 37; 46).

3.6 Voltage-Controlled Nano-Addressing Principle

The address line provides the gate voltage for the transistors. Each address line is connected to two external voltages at the ends (V_{dda1} and V_{ssa1} for address line 1, V_{dda2} and V_{ssa2} for address line 2). The position of a nanoscale wire in the array gives the gate voltage for the transistor

on the nanoscale wire alone the address line. For example, a i-th nanoscale wire (starting from V_{ss}) in an array of n equally spaced nanoscale wires has a transistor gate voltage

$$V_g(i,n) = \frac{i}{n}V_{dd} + \frac{n-i}{n}V_{ss} \tag{1}$$

in an address line connecting to two external voltage sources V_{dd} and V_{ss}. Here we assume uniform address lines of negligible external resistance (from the first or the last nanoscale wire to the nearest external voltage source).

A transistor is on if its gate voltage exceeds the threshold voltage $V_g > V_{th}$. A nanoscale wire is conductive if both transistors on it are on. Because the two address lines provide an increasing series and a decreasing series of gate voltages respectively, only nanoscale wires at specific positions in the array are conductive. For example, for $V_{dda1} = V_{dda2}$ and $V_{ssa1} = V_{ssa2}$, the nanoscale wire in the middle of the array gets conductive.

In general, to select the i-th data line from the left in an array of n nanoscale wires, the external voltages need to be such that all the transistors on the right hand side of the i-th data line in the first address line are off, and all the transistors on the left hand side of the i-th data line in the second address line are off:

$$\begin{aligned} V_{ga1}(i+1,n) &= (1-\frac{i+1}{n})V_{dda1} + \frac{i+1}{n}V_{ssa1} < V_{th} \\ V_{ga2}(i-1,n) &= \frac{i-1}{n}V_{dda2} + (1-\frac{i-1}{n})V_{ssa2} < V_{th} \end{aligned} \tag{2}$$

3.7 Voltage Controlled Nano-Addressing Analysis

Compared with the existing nano-addressing circuits, the proposed voltage-controlled nano-addressing circuit leads to significant manufacturing yield improvement due to the following reasons.

The existing nano-addressing circuits are based on binary decoders and require every nanoscale wire have a *unique physical structure* to differentiate itself, which is highly unlikely in a nanotechnology manufacturing process - lithography cannot achieve nanoscale resolution, while bottom-up self-assembly based nanotechnology manufacturing processes provide only regular structures. Even at microscale, such a structure is subject to prevalent catastrophic defects and significant parametric variations, which result in low yield.

On the contrary, the proposed circuit consists of only uniform components in a regular structure. Every nanoscale wire has a *uniform physical structure* and is *differentiated by their electrical parameters, e.g., the node voltages*. This scheme avoids any precise layout design and significantly improves yield and enables aggressive scaling of the addressing circuit with the rest of the nanoelectronic system.

Furthermore, let us compare voltage-controlled nano-addressing with the existing binary decoder based nano-addressing mechanisms in terms of addressing accuracy and resolution. These two key quantitative metrics for nano-addressing circuits are defined as follow since such definition is not available in previous publications to the best of the author's knowledge.

Definition 1. Addressing inaccuracy *of a nano-addressing circuit is the offset between the target data line i and the data line j of maximum current.*

$$AI = |i-j| \tag{3}$$

In voltage-controlled nano-addressing, addressing inaccuracy is given by inaccurate addressing voltages from the voltage dividers. Such addressing inaccuracy can be further minimized by adjusting the external voltages to adapt to manufacturing process and system runtime parametric variations. As a result, a mis-addressing is localized, i.e., the data line j of maximum current is not far from the target data line i.
In traditional binary decoder based nano-addressing, an n-bit binary address has n neighboring binary addresses of Hamming distance 1. A 1-bit error could lead to n different mis-addressings. This leads to non-localized mis-addressing and a more significant addressing inaccuracy.

Definition 2. Addressing resolution *of a nano-addressing circuit is the minimum ratio between the on current $I_{on}(i)$ of a target data line i and the off current $I_{off}(j)$ of a non-target data line j (under all conditions, e.g., different inputs and parametric variations).*

$$AR = Min\{\frac{I_{on}(i)}{I_{off}(j)}\} \tag{4}$$

In traditional binary decoder based nano-addressing, the achievable addressing resolution depends on the conductance difference between the target data line and other non-target data lines. There are n non-target data lines with Hamming distance 1 for a n-bit target address, which have similar if not identical conductances. The presence of parametric variations further reduces addressing resolution.
In voltage-controlled nano-addressing, addressing resolution is largely given by the addressing voltage difference between two adjacent data lines. Applying high voltages leads to a number of reliability issues, such as electromigration and gate dioxide breakdown. Carbon nanotubes are highly resistive to electromigration, while new material is needed to enhance reliability for gate dioxide breakdown.
Alternatively, for given gate voltage difference, transistor current difference can be improved by improving the inverse subthreshold slope. However, MOSFETs and MOSFET-like CNFETs are limited to an inverse subthreshold slope S (which is the minimum gate voltage variation needed to bring a $10\times$ source-drain current increase) of $2.3\frac{kT}{q} \approx 60mV/decade$ at $300K$ (46). This requires development of novel devices for larger inverse subthreshold slopes.

4. Adaptive Configuration of Nanoelectronic Systems Based on the CNT Crossbar Nano-Architecture

In this section, we examine a list of nanoelectronic design adaptive configuration methods which cancel the effects of catastrophic defects and parametric variations in the proposed CNT crossbar nano-architecture.

4.1 Adaptive Nano-Addressing

A variety of parametric variations are expected to be prevalent and significant in nanoelectronic systems. Their effects on the voltage-controlled nano-addressing circuit (Fig. 8) are as follow.

1. Global address line resistance variations, e.g., due to uniform width, height, and/or resistivity variations of the address lines, have no effect on the voltage divider hence the addressing scheme.
2. Address line misalignment (shifting) has no effect on the conductances of the data lines.

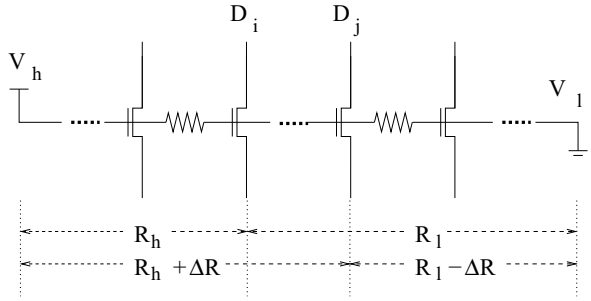

Fig. 9. Addressing two CNTs D_i and D_j with a resistance of ΔR in between.

3. Global data line misalignment (i.e., shifting of all data lines), variations of external voltage sources, and variations of external wire/contact resistance (between the resistive voltage divider and the external voltage sources) lead to potential addressing inaccuracy (CNT target offset).
4. Individual data line misalignment (shifting) could decrease the difference between the gate voltages of two adjacent transistors, leading to degraded addressing resolution (on/off CNT current ratio between two adjacent CNTs).
5. Process variations of the transistors, including width, length, dopant concentration, and oxide thickness variations, lead to transistor conductivity uncertainty and degraded addressing resolution.

The nano-addressing scheme needs to achieve a higher enough addressing resolution which endures the above-mentioned parametric variation effects (e.g., by applying high external addressing voltages, and/or novel CNFETs of $< 60mV/decade$ subthreshold slope).
After achieving satisfiable addressing resolution, we need to minimize any addressing inaccuracy and address the correct CNT data line (Problem 1).

Problem 1 (Adaptive Nano-Addressing)**.** *Given a voltage-controlled nano-addressing circuit, address the i-th CNT data line in the presence of parametric variations.*

Let us first derive the external voltage offset needed for a data address offset. Suppose for an address line, the external voltages V_h and V_l address the i-th CNT data line D_i. The resistance between CNT data line D_i and the high (low) external address voltage V_h (V_l) is R_h (R_l) (Fig. 9).[1] We have

$$\frac{R_l}{R_h + R_l} V_h + \frac{R_h}{R_h + R_l} V_l = V_{on} \tag{5}$$

where V_{on} is the voltage needed to address a CNT data line of peak current. Shifting the external voltages to $V_h + \Delta V$ and $V_l + \Delta V$ addresses another CNT data line D_j. The resistance between CNT data line D_j and the high (low) external address voltage is $R_h + \Delta R$ ($R_l - \Delta R$). We have

$$\frac{R_l - \Delta R}{R_h + R_l}(V_h + \Delta V) + \frac{R_h + \Delta R}{R_h + R_l}(V_l + \Delta V) = V_{on} \tag{6}$$

[1] For the first address line, the high external voltage $V_h = V_{l1}$ is on the left, the low external voltage $V_l = V_{r1}$ is on the right. For the second address line, the high external voltage $V_h = V_{r2}$ is on the right, the low external voltage $V_l = V_{l2}$ is on the left.

As a result,

$$\Delta V = \frac{\Delta R}{R_h + R_l}(V_h - V_l) \tag{7}$$

Observation 4. *The external voltage offset ΔV is proportional to the resistance offset ΔR between two CNT data lines, and is proportional to the physical offset ΔL between the two CNT data lines, if the resistive voltage dividers are uniform (e.g., the CNT data lines are equally spaced and the address lines have uniform resistivity).*

Based on Observation 1, Method 1 gives an adaptive nanoelectronic addressing method, which finds the external voltage shifts needed to address the left most and the right most CNT data lines first. Any other external voltage shift needed to address a specific CNT data line is then computed based on a linear interpolation. To address the left most or the right most CNT data line, we apply a gradually increasing/decreasing external voltage offset ΔV at an address line, keep all the transistors at the other address line on, and measure the conductance of the array of CNT data lines. The maximum and the minimum ΔV's (e.g., ΔV_{mink} and ΔV_{maxk}, $k = 1$ or 2) with non-zero CNT data line conductances address the left most and the right most CNT data lines, respectively.

Algorithm 1: Adaptive Voltage Controlled Nano Addressing

Input: An array of n CNT data lines, address i
Output: Addressing i-th data line

1. Turn on all transistors at address line 2 ($V_{l2} = V_{r2} > V_{th}$)
2. Find ΔV_{l1} which addresses first data line (binary search)
3. Find ΔV_{r1} which addresses n-th data line (binary search)
4. Turn on all transistors at address line 1 ($V_{l1} = V_{r1} > V_{th}$)
5. Find ΔV_{l2} which addresses first data line (binary search)
6. Find ΔV_{r2} which addresses n-th data line (binary search)
7. Shift V_{l1} and V_{r1} by $\frac{n-i}{n}\Delta V_{l1} + \frac{i}{n}\Delta V_{r1}$
8. Shift V_{l2} and V_{r2} by $\frac{n-i}{n}\Delta V_{l2} + \frac{i}{n}\Delta V_{r2}$

Observation 5. *The addressing accuracy given by Method 1 depends only on the uniformity of the resistive voltage divider, and the time domain variations of the external voltage differences $V_{l1} - V_{r1}$ and $V_{l2} - V_{r2}$. Any time-invariant (e.g., manufacturing process) variations of the external voltages (V_{l1}, V_{r1}, V_{l2}, and V_{r2}) or the external address line resistances (from the outer most data lines to the external voltage sources) do not affect the achievable addressing accuracy.*

4.2 RDG-CNFET Gate Matching

Another process variation is the misalignment of the front gate CNT and the back gate CNT of a reconfigurable double-gate CNFET (RDG-CNFET). This is because that the front gate CNT and the back gate CNT are on different ($i - 1$ and $i + 1$) layers, while CNT arrays on different layers do not have and are not expected to have a *precise* alignment mechanism.

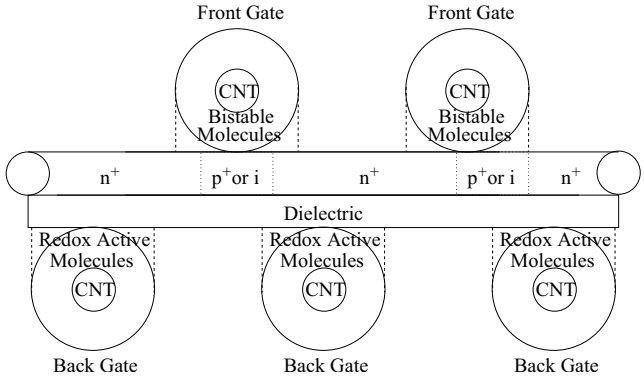

Fig. 10. CNT misalignment in dense CNT arrays. The closest CNT pair forms the front gate and the back gate of a RDG-CNFET. The neighboring CNTs have cross-coupling effect which needs to be simulated/tested or avoided by shielding.

Fortunately, we observe that precise alignment between a front gate CNT and a back gate CNT is not necessarily required as long as the CNT arrays are dense, e.g., with the spacing between CNTs close to the CNT diameters. In such a case, a double gate field effect transistor is formed even in the presence of CNT misalignment (Fig. 10). A CNFET channel is formed by doping the source/drain regions with the front gate CNT on the upper layer as mask. The resultant CNFET channel aligns with the front gate CNT. A misaligned back gate injects a weaker electrical field in the CNFET channel from a longer distance. A neighboring back gate may also injects a weak electrical field in the channel. This is either tolerated (which needs to be verified by simulation or testing) or avoided (by reserving the neighboring back gates for shielding).
The question is then how to find the closest CNT pair on different layers which form the front gate and the back gate of a RDG-CNFET (such that we can address them and configure the RDG-CNFET).

Problem 2 (RDG-CNFET Gate Matching)**.** *Given a CNT i on layer l, locate the closest CNT j on layer $l+2$ (or $l-2$) where CNTs i and j form the front gate and the back gate of a RDG-CNFET.*

Method 2 solves Problem 2 and finds the closest CNT pairs which form the front gate and the back gate of a RDG-CNFET.

Algorithm 2: RDG-CNFET Gate Matching

Input: CNT i on layer l which is a gate of CNFET T
Output: Closest CNT j to CNT i on layer $l+2$ ($l-2$) which is the other gate of CNFET T

1. Apply a turn-off gate voltage to CNT i
2. For each CNT j on layer $l+2$ ($l-2$),
3. Apply a turn-off gate voltage to CNT j
4. Measure the conductance of CNFET T
5. Find CNT j for the smallest CNFET conductance

Once a matching gate is identified, the CNFET can be characterized (by achieving its I-V curves). A parasitic CNFET can also be identified by finding the second closest CNT (with the second smallest CNFET conductance in the algorithm), which is either tolerated or avoided in a nanoelectronic design.

4.3 Catastrophic Defects and Mapping Techniques

In this subsection, we examine catastrophic defects for CNTs, programmable vias and CNFETs, and their corresponding detection and location methods.

4.3.1 Metallic, Open and Crossover CNTs

CNTs are metallic or semiconductive depending on their chirality. One third of CNTs are metallic if they are grown isotropically. Metallic CNTs can be removed by either chemical etching (64) or electrical breakdown (1). However, such techniques bring large process variation effects (34). Mitra et al. propose use of CNT bundles for each nanoelectronic signal to reduce metallic CNT effect (34). We observe that metallic CNTs need not necessarily to be removed and CNT bundles are not needed for each nanoelectronic signal as long as metallic CNTs can be detected and located. Upon detection and location, metallic CNTs can be configured to form global interconnects if not avoided. Their low resistivity helps to reduce signal propagation delay in global interconnects which are critical to nanoelectronic system performance.

Open CNTs are expected to be prevalent in a CNT array, as open CNT occurrence is proportional to the length of the CNT. A CNT with a single open can be largely included in a correct nanoelectronic design, upon detection and location of the single defect. A CNT with two (or more) opens is not fully utilizable. The segment between the two (extreme) opens are not accessible by any nano-addressing circuit, and components attached to that segment are not configurable. Upon detection and location of the extreme opens, the end segments of an open CNT can be included in a nano-circuit. Or, we can simply avoid open CNTs.

CNTs which are supposedly-parallel may cross over each other, resulting in different addresses for a CNT on two sides of a crossbar, and unexpected resistive contacts between CNTs. If not corrected by etching (34), such crossover CNTs can be taken as multi-thread cables and included in a correct nano-circuit. It is necessary to solve the following problem for nanoelectronic system configuration on a CNT crossbar nano-architecture.

Problem 3. *Detect and locate metallic, open and crossover CNTs in an CNT array, which are addressed on both ends by nano-addressing circuits.*