

Germanium Photodetector Technologies for Optical Communication Applications

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1. Introduction

Converging computing and communication capabilities on single chip platform is becoming increasingly important to keep up with the performance roadmap known as Moore's Law (Kimerling et al., 2006). Today, data transmissions at a bit-rate of 10 Gb/s over long distance makes photonic interconnection an easier approach to implement than electrical interconnect. At this data rate, the conventional copper solution has begun to encounter extreme challenges related to power consumption and reach (Wada et al., 2002). Moreover, the growing issues in electro-magnetic interference, signal cross-talk, and heavier weight make it an inferior approach for high bandwidth applications (Gunn, 2006). To keep up with the scaling of interconnect bandwidth, an alternative solution makes use of optical interconnect technology to meet the ever increasing bit rate requirement of data communication. Over the past decades, conventional optical components were typically made of exotic III-V compound materials such as gallium-arsenide (GaAs) and indium-phosphide (InP) due to their excellent light emission and absorption properties. Unfortunately, compound-semiconductor devices are generally too complicated to process and costly to implement in optical interconnects.

In search for a cost-effective solution, Si photonic emerges to hold great promise for its inexpensive material and its compatibility with current complementary metal-oxide-semiconductor (CMOS) process technology (Soref, 2006). However to make silicon photonic communication a reality, several key technological challenges have to be addressed. Inferior optical properties of Si have thus far the major show-stopper to preclude the development of a key active photonic component needed to perform optical to electrical encoding. Very recently, germanium (Ge) has attracted growing interest for the realization of high performance photodetector due to its favourable absorption coefficient (Hartmann et al., 2004). However, Ge can be a challenging material to integrate in a CMOS environment for its low thermal budget constraint and its large lattice mismatch of ~4.2% with Si (Luan et al., 1999). High defect densities seen in the Ge-on-Silicon-on-Insulator (Ge-on-SOI) epitaxial film could induce unfavourable carrier recombination process that would degrade the detector's quantum efficiency.

In this chapter, the current development of optical detection technologies on silicon photonics platform is reviewed. The discussion first begins with the development of Ge-on-

SOI hetero-epitaxy process technology. The approach, based on the low temperature pseudo-graded silicon-germanium buffer engineering, is adopted to relieve the large lattice mismatch of ~4.2% between the two heterostructure materials. This enables a high quality Ge epitaxy film with low threading dislocation density to be grown on Si. The subsequent sections of this chapter deal with the state-of-the-art Ge photodetector technologies. We begin with the discussion on the designs of evanescent-coupled Ge *p-i-n* photodetector featuring an integrated SOI micro-waveguide. Performance metrics in these detectors in terms of dark current, responsivity, and bandwidth are evaluated. The mechanism accountable for the leakage generation in such device and its dependence on the applied electric field strength are elucidated. Factors limiting the detector speed performance and guidelines to enable bandwidth scaling are also discussed.

This chapter also aims to discuss the demonstration of Schottky barrier engineered Ge photodetector featuring metal-semiconductor-metal (MSM) configuration. The problem and mechanism responsible for the generation of high leakage current in such a detector are dealt with. Novel concepts adopted to address this issue through Schottky barrier modulation are presented. The approaches are based on bandgap engineering as well as Fermi level de-pinning by segregating valence mending adsorbate near the metal/germanium interface. The recent technological breakthrough in employing all Group-IV based materials to realize high gain-bandwidth product Ge/Si avalanche photodetector (APD) is presented next. The fabrication process and the design of Ge/Si APD featuring separate-absorption-charge-multiplication (SACM) configuration are discussed. We conclude the chapter with a summary providing the readers with the comparative views on the performance metrics of the various Ge-based photodetector schemes.

2. Hetero-Epitaxy of Germanium on Silicon

The key challenge to high quality germanium (Ge) epitaxy growth on silicon (Si) rests with the huge lattice mismatch between the two heterostructure materials. The existence of ~4.2% lattice mismatch strain has been shown to give rise to two major issues: (1) high densities of threading dislocations and (2) rough surface morphology due to 3D Stranski-Krastanov (SK) growth. Both of these defects present much concerns for the generation of high leakage current which would compromise the efficiency of a photodetector. Strategies proposed in the literature to overcome these challenges vary to a large extent. One most intuitive approach is to grow a silicon-germanium (SiGe) layer by compositionally grading its Ge concentration up to 100%. Using low-energy plasma enhanced chemical vapour deposition, Oh et al. (2002) showed that for every 10% increase in the Ge mole fraction, a linearly graded SiGe buffer of ~1 μm thickness is required. This results in a need to grow a relatively thick SiGe buffer layer of 10 μm before a low dislocation density Ge epilayer can be deposited, which imposes much difficulties for process integration.

In an effort to further reduce the thickness of these active layers, Huang et al. (2004) proposed another approach based on the optimization of two thin SiGe buffer layers with varying Ge concentration. In such approach, a 0.6 μm thick Si_{0.45}Ge_{0.55} buffer was first grown and then followed by an intermediate Si_{0.35}Ge_{0.65} buffer with a thickness of 0.4 μm . An in-situ annealing for 15 min at 750°C was subsequently performed to further reduce the dislocation density before the growth of a 2.5 μm thick Ge epilayer at a process temperature of 400°C. Through this approach, it allows the threading dislocations to be trapped at the hetero-

interfaces. This enables a significant reduction in the dislocation density of the as-grown Ge epilayer, thereby improving the detector's dark current performance.

In yet another approach, Colace et al. (1999) proposed a direct hetero-epitaxy growth of Ge on Si through the use of a low temperature thin SiGe buffer layer (a few 10nm). The insertion of such thin buffer avoids the occurrence of 3D SK growth, and allows the misfit dislocations to be concentrated at the hetero-interfaces. However such approach requires a cyclic annealing process to be carried out at both high and low temperature (900°C/780°C) to reduce the threading dislocation density within the Ge active film. Using a similar cyclic thermal annealing approach, Luan et al. (1999) had also demonstrated a significant improvement in both the surface roughness and the dislocation density. When combined with the selective area growth, an average threading dislocation density as low as $2.3 \times 10^6 \text{ cm}^{-2}$ was achieved. However, the needs for a high temperature post-epitaxy Ge anneal with long cycle time present a major concern for CMOS implementation.

In this work, selective epitaxial growth of Ge on silicon-on-insulator (SOI) was performed using an ultra-high vacuum chemical vapor deposition (Ang et al., 2010) reactor. Unlike the conventional approaches, a thin pseudo-graded SiGe buffer with a thickness of $\sim 20\text{nm}$ is proposed in this study to relieve the large lattice mismatch stress between the two heterostructure materials (Fig. 1). The Ge mole fraction within the SiGe buffer is compositionally graded from 10% to $\sim 50\%$. The precursor gases used for the SiGe growth comprise of diluted germane (GeH_4) and pure disilane (Si_2H_6). A relatively thin Ge seed layer of $\sim 30\text{nm}$ is subsequently grown on the SiGe buffer at a process temperature of 370°C . The use of a low temperature growth is intended to suppress adatoms migration on Si and thus prevents the formation of 3D SK growth, which allows a flat Ge surface morphology to be achieved. Upon obtaining a smooth Ge seed layer, the epitaxy process temperature is then increased to $\sim 550^\circ\text{C}$ to facilitate faster epitaxy growth to obtain the desired Ge thickness. Using this approach, high quality Ge epilayer with a thickness of up to $\sim 2\mu\text{m}$ has been demonstrated, along with the achievement of threading dislocation density as low as $\sim 10^7 \text{ cm}^{-2}$ without undergoing any high temperature cyclical thermal annealing step.

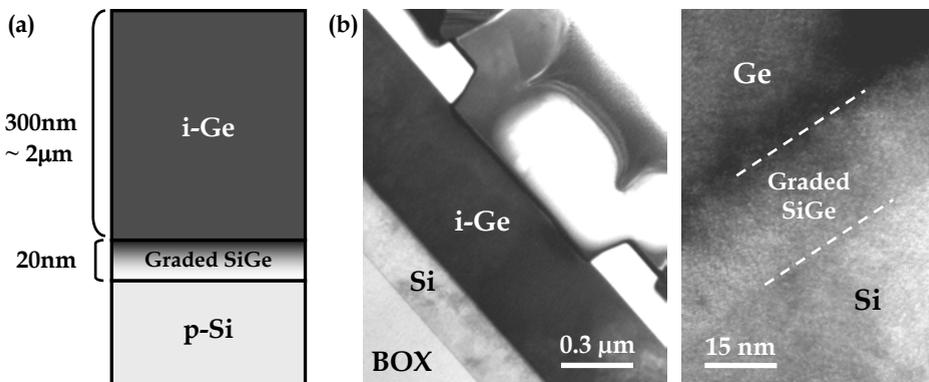


Fig. 1. (a) Schematic view of the layer stack for the direct hetero-epitaxy growth of Ge on Si. (b) High resolution TEM micrograph showing the effectiveness of a pseudo-graded SiGe buffer in reducing the threading dislocation density within the Ge epilayer.

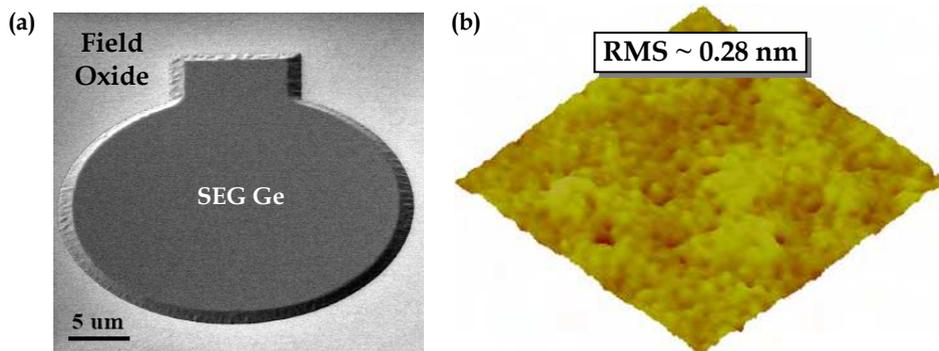


Fig. 2. (a) Scanning electron microscopy (SEM) image showing the achievement of excellent Ge epitaxy growth and selectivity on SOI substrate. (b) Excellent Ge surface roughness of $\sim 0.28\text{nm}$ was achieved, as determined using atomic force microscopy (AFM).

In addition, selective area growth of Ge on Si has also been developed using a cyclical deposition and etch back approach. In each deposition cycle, the Ge growth time is carefully optimized to avoid exceeding the incubation time needed for Ge seeds to nucleate on the dielectric film. After every Ge deposition cycle, a short etch back process using chlorine (Cl_2) precursor gas will then be introduced to remove possible Ge nucleation sites on the dielectric. This allows a highly selective Ge epitaxy process to be developed, along with the achievement of excellent surface roughness of $\sim 0.28\text{nm}$ (Fig. 2).

3. High Performance Germanium *p-i-n* Photodetector

Due to its poor absorption coefficient as inherited by the large bandgap energy, silicon (Si) has been known to be prohibitive for the realization of photodetector that is capable of performing efficient optical detections at wavelengths commonly used in optical fiber communication ($1.31\sim 1.55\mu\text{m}$). This can be addressed by introducing a new material with a smaller bandgap energy such as germanium (Ge) to provide favorable optical absorption property at these wavelengths. Recent research progress made in the photodetector technology development has clearly shown that Ge is attracting growing interest as the preferred photo-absorbing material due to its much higher absorption coefficient as compared to that of Si (Hartmann et al., 2002). In addition, its compatibility with current CMOS fabrication technology makes it an attractive material to enable the demonstration of high performance near-infrared photodetector (Soref, 2006).

However, the long absorption length in Ge at $1.55\mu\text{m}$ wavelength renders it difficult to meet the high quantum efficiency requirement for a surface illuminated photodetector. Despite the use of a $\sim 1\mu\text{m}$ Ge active layer, Colace et al. (2007) reported the achievement of a maximum responsivity of merely 0.2A/W at $1.55\mu\text{m}$ wavelength. One way to overcome this constraint requires the growth of a thick Ge epilayer to enable full absorption at this wavelength. Unfortunately, hetero-epitaxy of Ge with such thickness imposes much process integration challenge such as high threading dislocation densities that would lead to increased leakage current and thus degrade the receiver sensitivity. An alternative approach to relax this requirement makes use of a waveguide based photodetector (Yin et al., 2007).

By leveraging on the detector length, one would be able to achieve enhanced photo-detection efficiency and thus responsivity improvement. In addition, the bandwidth performance of the photodetector can also be simultaneously optimized by tweaking the Ge thickness to reduce the carrier transit time delay.

In this section, the different designs of waveguide integrated Ge photodetector featuring *p-i-n* configuration are discussed. The performance metrics such as dark current, responsivity, and bandwidth in these devices are evaluated and compared.

3.1 Ge-on-SOI Photodetector Designs and Fabrication

Two types of evanescent butt-coupled Ge-on-SOI photodetector design are shown in Fig. 3. Photodetectors featuring vertical *p-i-n* (VPD) and lateral *p-i-n* (LPD) configurations were fabricated, with Ge active layer selectively grown and integrated on a SOI micro-waveguide. For the VPD, the p+ and n+ junctions were formed in the Si and Ge regions, respectively, with the intrinsic region thickness (t_{i-Ge}) co-defined by the Ge thickness (t_{Ge}) and the thickness of the n+ implant region [Fig. 3(a)]. The width W and length L of this VPD design is $8\mu\text{m}$ and $100\mu\text{m}$, respectively. For the LPD design, both the p+ and n+ junctions were formed in the Ge region, with the width of the intrinsic region (w_{i-Ge}) determined by defining the spacing of these alternating contacts [Fig. 3(b)]. Note that the width W and length L of this LPD design is $20\mu\text{m}$ and $100\mu\text{m}$, respectively.

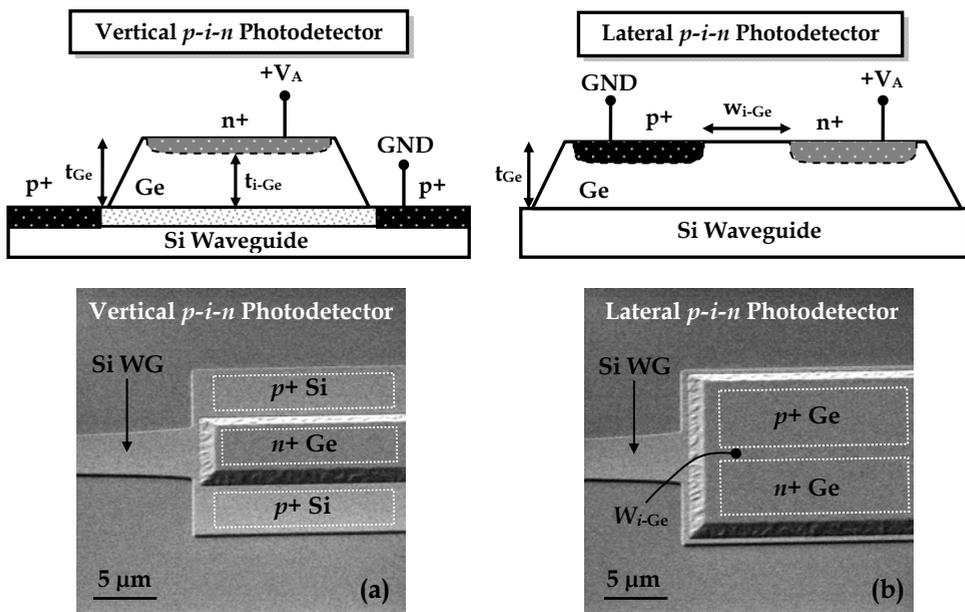


Fig. 3. (a) SEM micrograph showing the design of an evanescent butt-coupled Ge photodetector featuring vertical *p-i-n* configuration. (b) Ge photodetector design with a lateral *p-i-n* configuration.

By employing a waveguide-coupled design, the requirement for thick Ge epilayer to enhance the responsivity performance can be greatly relieved as one can leverage on the detector length to improve the optical absorption efficiency. As a result of the difference in the refractive index between Si and Ge, the incident photon traveling in the SOI micro-waveguide will be up-coupled into the Ge absorbing layer to allow optical signal to be encoded into its electrical equivalent efficiently. The insertion of a thick buried oxide (BOX) of $\sim 2\mu\text{m}$ serves to confine the optical mode within the core of the channel waveguide so as to prevent leakage into the underneath Si substrate.

The fabrication process of the waveguide integrated Ge photodetector begins with the use of SOI substrate with a starting overlying Si thickness of $\sim 220\text{nm}$ and a buried oxide (BOX) thickness of $\sim 2\mu\text{m}$. Channel waveguide with a nano-taper featuring a width of $\sim 200\text{nm}$ was first formed by anisotropic dry etching to obtain a smooth sidewall profile for enabling low waveguide propagation loss. Ion implantation employing boron species was selectively done to form the Si anodes in a VPD detector. A moderately high p-type doping concentration was carefully chosen for the anode formation to ensure low series resistance while not impact the quality of the as-grown Ge epitaxy film. High dose p+ contact implant was subsequently performed and dopants are activated using rapid thermal anneal at 1030°C for 5s to obtain good Si ohmic contacts. After depositing a 600\AA thick field oxide as passivation layer, a combination of anisotropic dry etch and followed by wet etch approach was adopted to preserve the top Si surface quality from possible damage by the reactive ion etching process. Hetero-epitaxy of Ge was then selectively grown in an ultra-high vacuum chemical vapor deposition (UHVCVD) epitaxy reactor. The selective Ge epitaxy process commenced with the deposition of a low temperature pseudo-graded silicon-germanium buffer ($\sim 20\text{nm}$) and followed by a Ge seed layer with a thickness of $\sim 30\text{nm}$. A cyclical deposition and etch back approach was then used to raise the Ge thickness to $\sim 500\text{nm}$. Due to the achievement of low defects level within the Ge film, the high temperature post-epitaxy Ge anneal typically used for defects annihilation was skipped to reduce the overall thermal budget. High dose selective phosphorous and boron implants were then performed in a LPD and annealed at 500°C for 5 min to form good n-type and p-type Ge ohmic contacts, respectively. After the deposition of inter-layer dielectric (ILD), contact and metallization were subsequently done to complete the device fabrication. Fig. 3(a) and 3(b) show the top-view scanning electron microscopy (SEM) images of the VPD and LPD detectors, respectively.

3.2 Dark Current Characteristics

Dark current plays a vital role in affecting the shot noise (I_S) in a photodetector according to the following expression

$$I_S^2 = 2 q B (I_D + I_B) \quad (1)$$

where q denotes the elemental charge, B the bandwidth, I_D the dark current of the detector, and I_B the photocurrent due to background radiation. Under a carefully controlled situation, I_B is usually small and can therefore be neglected. However, thermal generation and/or defects-assisted tunnelling current due to strong electric field give rise to considerable dark current which degrades the shot noise and thus affects the signal-to-noise (SNR) ratio.

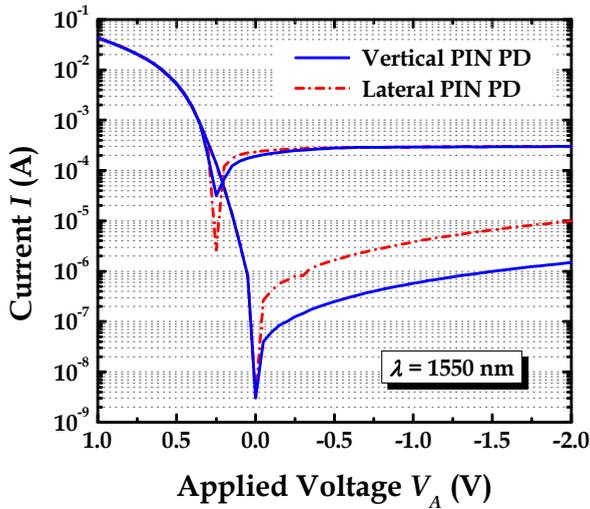


Fig. 4. The current-voltage characteristics of the VPD and LPD detectors measured under dark and illumination conditions.

Fig. 4 examines the current-voltage characteristics of the VPD and LPD detectors under dark and illumination conditions. Excellent rectifying characteristics were demonstrated in both the detectors, showing a forward-to-reverse current ratio of ~4 orders of magnitude. For a given applied bias of -1.0V, the dark current (I_{dark}) in a VPD was measured to be ~0.57μA (or ~0.7nA/μm²), which is below the typical 1.0μA generally considered to be the upper limit for high speed receiver design. On the other hand, the dark current performance in a LPD showed a much higher I_{dark} value of ~3.8μA (or ~1.9nA/μm²). In order to better understand the factors which affect the dark current density (J_{Dark}), let us review the expression that governs the leakage generation in a semiconductor diode

$$J_{Dark} = \frac{qn_i d}{\tau_{eff}} \tag{2}$$

where q denotes the elemental charge, n_i the intrinsic carrier density, d the depletion layer width, and τ_{eff} the effective carrier lifetime. Clearly, an increase in the depletion layer width leads to a detrimental impact on the dark current performance, which could possibly explain the higher I_{dark} experienced in a LPD detector. In addition, it is also important to note that I_{dark} exhibits a strong dependence on the effective carrier lifetime which is controlled by both the lifetime associated with the Shockley-Read-Hall recombination (τ_{SRH}) and the carrier drift time across the space charge region (τ_{drift}) as follow

$$\frac{1}{\tau_{eff}} = \frac{1}{\tau_{SRH}} + \frac{1}{\tau_{drift}} \tag{3}$$

$$\tau_{SRH} = \frac{1}{\sigma v_{th} N_{TD} N_D} \quad (4)$$

$$\tau_{drift} = \frac{d}{\mu E} \quad (5)$$

where σ denotes the capture cross section, v_{th} the carriers thermal velocity, N_{TD} the threading dislocation density, N_D the density of recombination centres, μ the low-field carrier mobility and E the electric field strength. It is obvious that the reverse dark current density should be proportional to the defects density within the Ge epilayer and a careful control of the epitaxy quality would be important to reduce the leakage current. Furthermore, an increase in the applied reverse bias has also resulted in an aggravated dark current degradation, which elucidates that I_{dark} has a strong dependence on the electric field strength. A further analysis on this phenomenon will be covered in a later discussion (see section 3.5).

3.3 Responsivity Characteristics

The responsivity (\mathfrak{R}) of a photodetector can be described using the following expression

$$\mathfrak{R} = I_{Photo} / P_{Opt} = \eta q / h\nu \quad (6)$$

where I_{Photo} denotes the photocurrent, P_{Opt} the incident optical power, η the quantum efficiency, q the elemental charge, h the Planck constant, and ν the frequency. In general, the incident photons which are absorbed in germanium generate electron-hole pairs which will be collected as photocurrent under applied electric field. This photocurrent is linearly dependent on the incident optical power before saturation is reached. Moreover, alike the quantum efficiency, the responsivity of the detector should be wavelength dependent. Hence, the responsivity of a detector will be significantly higher at wavelength where the photon energy enables electron-hole pair generation through direct transition.

In order to compare the responsivity performance between the VPD and LPD, optical measurements were performed by injecting an incident photon with a wavelength of 1550nm into the SOI micro-waveguide. The typical optical propagation loss in our SOI micro-waveguide under TE polarization mode is ~ 2 dB/cm. No coupler was integrated with the Si waveguide and the incidence light was coupled through a single mode lensed fiber directly into the Si nano-taper. For an incident light power of $\sim 300\mu W$, optical measurements showed that both the VPD and LPD detectors achieved a comparable photocurrent level at high applied biases beyond -1.0V. Fig. 5 compares the responsivity of the detectors as a function of the applied voltages. It is interesting to note that the vertical PIN detector demonstrated a lower responsivity as compared to the lateral PIN detector for biases below -0.5 V. This could possibly be due to an enhanced carrier recombination process at the high density of defect centres near the Ge-Si heterojunction. This is set to compromise the absolute photocurrent value of a vertical PIN detector under low field influence. However with an increased electrostatic potential across the depletion layer, the photo-generated carriers can be assisted across the space charge region with enhanced mobility before they can recombine at these recombination centres.

For an applied bias larger than -1.0 V, a comparable responsivity was measured for both the vertical and lateral PIN detectors. Despite that the metallurgical junction is separated by merely $0.8\mu\text{m}$, a lateral PIN detector showed a high absolute responsivity of ~ 0.9 A/W. The possible mechanisms accountable for such high responsivity could be attributed to the following reasons. Firstly, under high reversed bias, the intrinsic Ge region (i.e. between and beneath the metallurgical junction) was simulated to be totally depleted, as confirmed using MEDICI device simulator. When photon is absorbed to produce electron and hole pairs, the fringe field beneath the metallurgical junction enables the generated carriers to be collected by the electrode as photocurrent. Secondly, optical simulation shows that more than 80% of the incidence light travelling in the SOI waveguide is absorbed within the first $25\mu\text{m}$ of the detector. Hence by leveraging on the long absorption length design, nearly all incidence photons will be expected to contribute to the achievement of high responsivity.

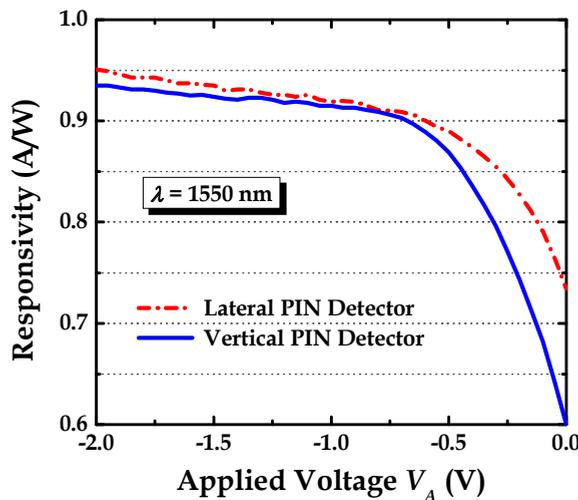


Fig. 5. Responsivity as a function of applied voltages for both the VPD and LPD detectors measured at a wavelength of 1550nm.

3.4 Impulse Response Characteristics

The impulse response of a photodetector is limited by both the carrier transit time ($f_{Transit}$) and the RC time constant (f_{RC}) which can be modelled using the following expressions

$$f_{Transit} = \frac{0.45 v_{sat}}{t_{i-Ge}} \tag{7}$$

$$f_{RC} = \frac{1}{2\pi RC} \tag{8}$$

where v_{Sat} denotes the carrier saturation velocity, d the depletion layer width, and RC the resistances and capacitances associated with the detector and its peripheral circuitry.

As described in these equations, the factors governing the fundamental response time limit of a detector lie with (1) the carrier drift time across the space charge region, and (2) the device junction capacitance. Drift of carriers is influenced by the electric field applied across the space charge region and can be expressed using

$$v_{\text{drift}} = \mu \cdot E \quad (9)$$

where μ denotes the carrier mobility, and E the electric field. Clearly, increasing the electric field would enhance the drift velocity across the space charge region until a saturation velocity is reached. Sze (1981) showed that the carrier saturation velocity in germanium is on the order of $\sim 10^7$ cm/s. In addition, the higher carrier mobility in Ge as compared to that of Si makes it a material of choice to enable the realization of high speed photodetector. On the other hand, decreasing the junction capacitance would allow one to achieve a reduced RC time constant. The junction capacitance (C_j) which arises from the ionized donors (N_D) and acceptors (N_A) is expressed as follow

$$C_j = \epsilon A \left[\frac{q}{2\epsilon(V_o - V)} \frac{N_D N_A}{N_D + N_A} \right]^{1/2} = \frac{\epsilon \cdot A}{W} \quad (10)$$

where ϵ denotes the material permittivity, A the cross-sectional area of the detector, and W the depletion layer width. Intuitively, reducing the device area and increasing the depletion layer width are both beneficial to reduce the junction capacitance. However, adopting the former approach could lead to a compromise in the responsivity performance as the effective area for optical absorption is decreased. The latter approach in enlarging the depletion width could serve to enhance the response time as a result of lower junction capacitance. However, further increase in the depletion width would eventually lead to a degraded transit time across the space charge region. Therefore, an optimization of the RC time constant and the carrier transit time will be crucial in determining the overall bandwidth performance of the detector, as dictated using the following expression

$$f_{3\text{dB}} = \sqrt{\frac{1}{1/f_{\text{Transit}}^2 + 1/f_{\text{RC}}^2}} \quad (11)$$

In order to investigate the factors affecting the speed performance of the VPD and LPD detectors used in this study, impulse response measurements were performed at a photon wavelength of 1550nm. A pulsed laser source having a 80fs pulse width was used in the measurements. Both the detectors were characterized using microwave probes and the impulse responses were captured with a high speed sampling oscilloscope. Fig. 6 shows that a VPD detector achieved a smaller full-width-at-half-maximum (FWHM) pulse width of ~ 24.4 ps as compared to that of LPD detector with a slightly larger FWHM of ~ 28.9 ps. This could be attributed to the smaller depletion layer width design in a VPD detector which reduces the carrier transit time. The FWHM pulse width is related to the bandwidth and can be used as a metric to gauge the speed performance of the detectors. By performing a fast Fourier transform of the impulse responses, a -3dB bandwidth of ~ 11.3 and ~ 10.1 GHz were achieved in the VPD and LPD detectors, respectively.

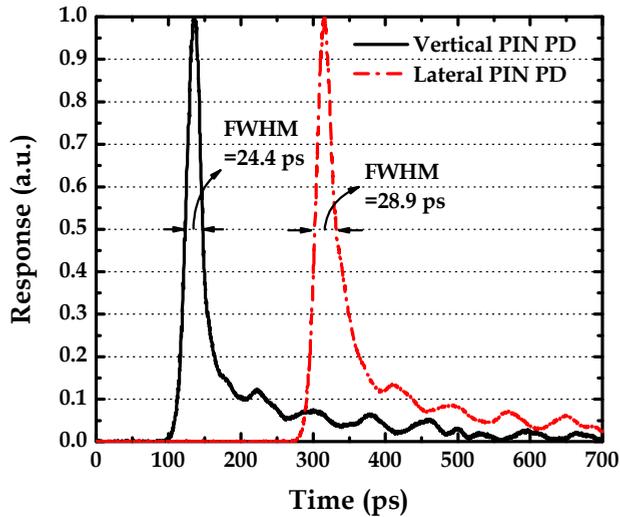


Fig. 6. Impulse responses of the VPD and LPD detectors measured at a wavelength of 1550nm. A smaller FWHM pulse width of ~ 24.4 ps was achieved in a VPD as compared to a LPD, which corresponds to a -3 dB bandwidth of ~ 11.3 GHz.

The detector's bandwidth can be further evidenced by the eye patterns measurements (PRBS 2⁷-1) done by directly connecting the output of the detector to the 50 Ω electrical input of the DCA. Fig. 7 shows that high sensitivity and low-noise photo-detection up to a bit-rate of 8.5Gb/s can be achieved by the VPD detector. The clean eye patterns clearly illustrate the low noise property of the detector. Higher speed measurements are possible through further scaling of the detector geometry to reduce the device capacitance.

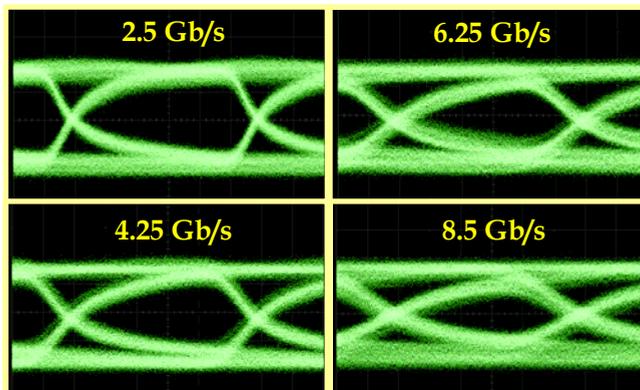


Fig. 7. Eye patterns (PRBS 2⁷-1) measurements of the VPD at a bias of -1.0 V. The detector demonstrated high sensitivity and low-noise photodetection up to a bit-rate of 8.5Gb/s. The low noise property of the detector can be clearly illustrated by the clean eye patterns.

Fig. 8(a) shows the total device capacitance measured as a function of the applied reverse voltages for different detector geometry. Obviously, elongating the detector length increases the capacitance due to a larger effective detector area, as predicted in equation (9). Moreover, in the presence of increased reverse bias, the capacitance drops drastically and nearly plateaus off at high voltage regime. This is attributed to the widening of the depletion layer width as the applied bias is raised. Further increase in the bias across the alternating p+ and n+ junctions would lead to a total depletion of the intrinsic-Ge region, which causes the device capacitance to reach a saturation level.

The theoretical modelling results of the RC-time constant and the transit-time bandwidth are plotted in Fig. 8(b). Reducing the depletion spacing enhances the transit-time bandwidth performance significantly, but it leads to a degraded RC-time bandwidth. To overcome this limitation, one could scale the detector length to achieve lower capacitance for bandwidth improvement.

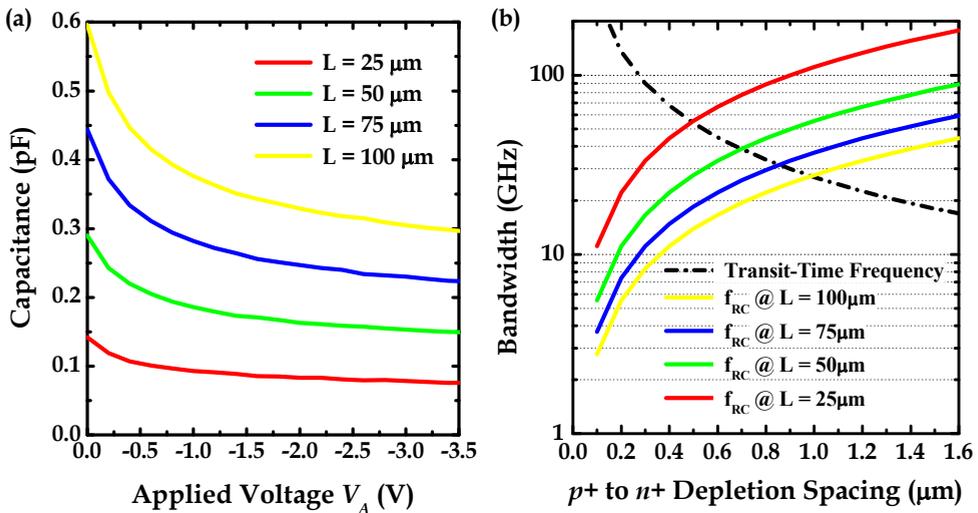


Fig. 8. (a) Measured capacitance as a function of applied voltage for Ge photodetector with various detector lengths. (b) Downscaling of detector length results in bandwidth enhancement due to a reduced device capacitance.

3.5 Impact of Band-Traps-Band Tunneling on Dark Current Generation

In order to gain insight into the leakage mechanism for the Ge detectors, an activation energy analysis of the dark current I_{Dark} was performed (Ang et al., 2009). In this analysis, the I_{Dark} can be modelled using the following functional form

$$I_{Dark} = BT^{3/2} e^{-E_a/kT} (e^{eV_a/2kT} - 1) \tag{12}$$

where T denotes the temperature, V_a the applied bias, and E_a the activation energy responsible for the leakage generation. Fig. 9(a) plots the bias dependence of dark current in a Ge p-i-n photodetector measured at increasing temperature range from 303K to 373K. As

can be observed from this figure, temperature has a significant impact on I_{Dark} . Increasing the operating temperature and the applied bias are found to result in a higher I_{Dark} . The applied bias V_A used in this measurement ranges from -1.5V to +0.2V.

A semi-log plot of I_{Dark} as a function of $1/kT$ at various reverse bias voltages is shown in Fig. 9(b). A straight line fitting to this plot yields a gradient which corresponds to the activation energy E_a . At a fixed reversed bias of -0.5V, the extracted E_a is observed to be nearly half of the Ge bandgap energy E_g , which elucidates that the dark current mechanism is dominated by the Shockley-Read-Hall (SRH) process via deep levels in the Ge forbidden gap (Shockley & Read, 1952). This is not all unexpected as the large lattice mismatch between the two heterostructure materials could result in a Ge epitaxial film with high threading dislocation density. The existence of such defects has been shown to affect the effective carrier lifetime which causes an increase in the leakage current, as discussed earlier in Section 3.2.

Interestingly, the analysis also reveals a strong dependence of E_a on the electric field strength, as illustrated in Fig. 10(a). Increasing the field intensity across the depletion region is shown to result in a decreasing E_a responsible for the leakage generation. This in turn, contributes to an exponential increase in the dark current trend. The mechanism responsible for this is that electric field enlarges the band-bending which leads to an enhanced electrons and holes tunnelling from the resulting deep levels into the respective conduction and valence bands, thereby contributing to the dark current degradation. For instance, an increase in the electric field strength from 17kV/cm to 25kV/cm enhances the dark current from 0.27 μ A to 0.44 μ A, showing more than 60% I_{Dark} degradation.

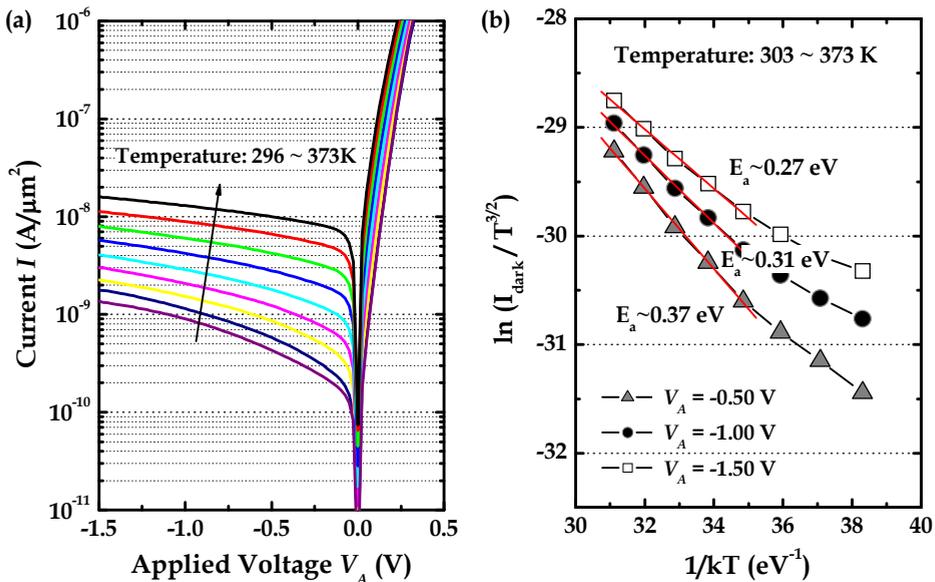


Fig. 9. (a) Plot of dark current characteristics as a function of applied bias for a Ge p-i-n photodetector with increasing temperature range from 303 K to 373 K. (b) An extraction of the activation energy for leakage generation as a function of applied bias.

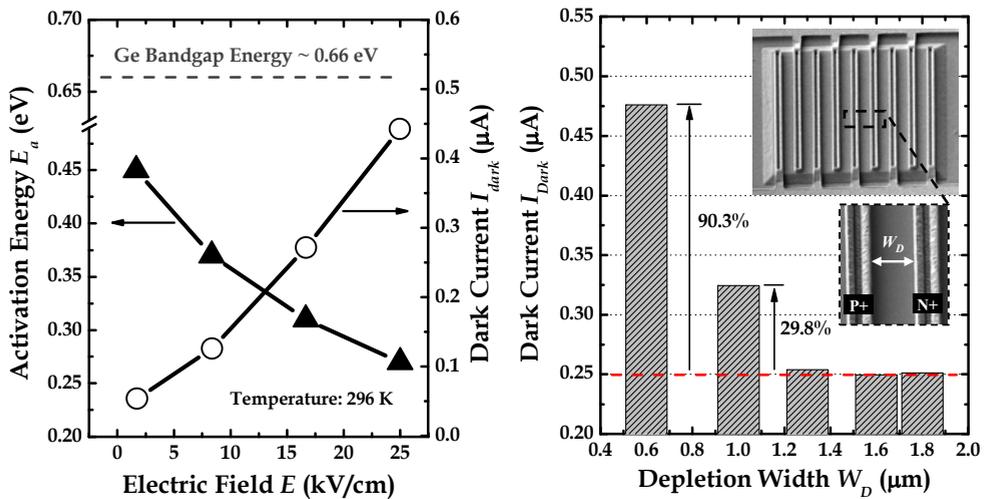


Fig. 10. (a) The activation energy E_a for leakage generation shows a strong dependence on the applied electric field, giving rise to a decreasing E_a trend with increasing field intensity. A reduced E_a at high field regime leads to an increased dark current generation. (b) Plot of dark current dependence on depletion width W_D of a Ge p-i-n photodetector. Scaling W_D leads to significantly higher dark current generation.

Such band-traps-band tunneling effect is observed to demonstrate a strong dependence on the depletion width W_D which separates the p+ and n+ metallurgical junctions. In this analysis, the area of the Ge detector is kept constant at $23 \times 23 \mu\text{m}^2$ while the W_D is varied from $0.6\text{--}1.8 \mu\text{m}$. To avoid a difference in the contact area due to a variation of intrinsic Ge width, the metal geometry is also altered such that the total metal contact region is comparable for all designs. Note that a reduced W_D is often desirable from the perspective of enhancing the detector's bandwidth performance. Fig. 10(b) shows that an aggressive downsizing of W_D results in a significant dark current degradation. Specifically, a reduction of W_D from $1.3 \mu\text{m}$ to $1.0 \mu\text{m}$ increases the dark current density by $\sim 29\%$, which is further aggravated to $\sim 90\%$ when W_D reaches $0.6 \mu\text{m}$.

The underlying mechanism responsible for such phenomenon can be explained using the band diagrams as shown in Fig. 11. When operated in the high field regime, enlarged band-bending results in a more prominent Ge bandgap narrowing for a detector with an aggressively scaled W_D [Fig. 11(a)]. As a consequence, the occurrence of electrons and holes tunnelling from the resulting mid-gap trap levels could be further enhanced in the presence of strong electric field, which accounts for the achievement of higher dark current over a detector with wide W_D [Fig. 11(b)]. It is also noteworthy to highlight that the dark current density begins to plateau for $W_D > 1.3 \mu\text{m}$, which implies that the influence of band-traps-band tunnelling on the leakage generation becomes relatively less prominent for wider W_D . This finding suggests that a design trade-off needs to be considered in the course of scaling W_D for enabling bandwidth enhancement as it would lead to a more pronounced dark current degradation.

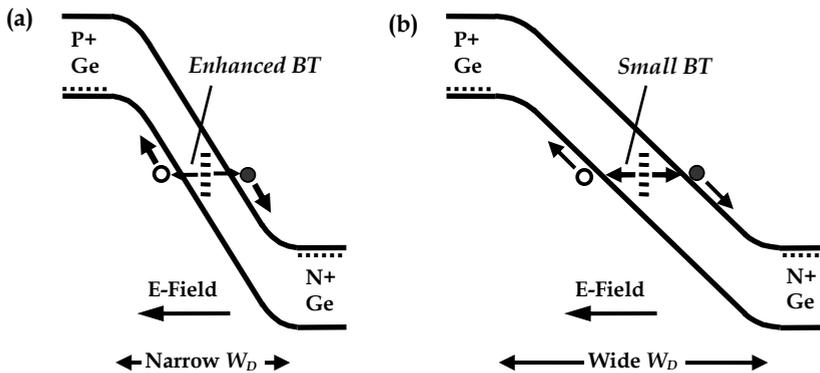


Fig. 11. Band diagrams illustrating the impact of scaling depletion width W_D on field-enhanced dark current generation. When operated at high field regime, enlarged band-bending results in a narrowing of Ge bandgap which enables electrons and holes tunnelling to occur via these defect centres. Such phenomenon is observed to become increasingly prominent for devices with (a) narrow W_D as compared to that with (b) wide W_D .

4. Schottky Barrier Engineered Germanium MSM Photodetector

In another photodetector scheme, a metal-semiconductor-metal (MSM) structure was utilized to leverage on the advantage of low capacitance and ease of process integration. However, high dark current issue experienced in these detectors imposes much concern for the achievement of poor signal-to-noise (SNR) ratio. This drawback would be further aggravated when a narrow bandgap material such as Ge is employed, where high dark current is predominantly attributed to the low hole Schottky barrier height as a result of Fermi level pinning near the valence band edge. Recent experimental demonstration showed that Ge MSM photodetector with an integrated SOI rib waveguide exhibited high dark current on the order of $150\mu\text{A}$ despite achieving impressive speed performance (Vivien et al., 2007). Such dark current level is way too high to be acceptable for high speed receiver design which typically tolerates a leakage current below $1.0\mu\text{A}$.

This chapter aims to deal with this problem through the application of novel approaches to suppress the leakage current in Ge MSM photodetector. The concepts are based upon Schottky barrier modulation through bandgap engineering as well as Fermi level de-pinning by segregating valence mending adsorbate at the metal/germanium interface.

4.1 Schottky Barrier Modulation using Large Bandgap Material

The application of larger bandgap material for Schottky barrier modulation has been widely pursued to enable dark current suppression in Ge MSM photodetector. Oh et al. (2004) reported the fabrication of metal-Ge-metal photodetector featuring thin amorphous-Ge layer sandwiched between the metal and germanium interface to increase the Schottky barrier height. Using this approach, a substantial reduction of dark current by more than two orders of magnitude was achieved. Laih et al. (1998), on the other hand, adopted an amorphous-Si layer in a U-grooved metal-semiconductor-metal photodetector to enable

dark current suppression by more than three orders of magnitude. In this work, a novel crystalline silicon-carbon (Si:C) epilayer was proposed for modulating the Schottky barrier height in a Ge MSM photodetector with an integrated SOI micro-waveguide.

The fabrication process begins with an 8-inch silicon-on-insulator (SOI) substrate with (100) surface orientation. The SOI substrate features a silicon body thickness of ~ 250 nm and a buried oxide thickness of ~ 1 μm . Si micro-waveguide was first formed by using anisotropic dry etching to achieve straight sidewall profile for enabling low propagation loss. After depositing a 120nm plasma enhanced chemical vapor deposition (PECVD) oxide as passivation layer, the Ge active regions were then patterned by reactive ion etching and cleaned with standard piranha solution (i.e. a mixture of sulfuric acid (H_2SO_4) with hydrogen peroxide (H_2O_2) for polymer removal. The wafers were subsequently cleaned with standard SC1 ($\text{NH}_4\text{OH} : \text{H}_2\text{O}_2 : \text{H}_2\text{O}$) and then subjected to a HF-last wet cleaning for oxide removal prior to the selective epitaxial growth of Ge in an ultra high vacuum chemical vapor deposition (UHVCVD) system. The epitaxy growth started with an in-situ baking in N_2 ambient at 800°C for native oxide removal and followed by the deposition of a ~ 5 nm thin Si buffer at 530°C . A thin SiGe buffer layer was then deposited to have a gradual transition from pure Si to pure Ge at the hetero-interface. A Ge seed layer with a thickness of ~ 30 nm was then grown using low temperature at 370°C before the growth of a ~ 300 nm Ge epilayer at increased temperature. Precursor gases comprise of pure disilane Si_2H_6 and diluted germane GeH_4 (10% GeH_4 : 90% Ar) were employed for the hetero-epitaxy growth of SiGe and Ge layers. The defects density within the Ge epilayer was measured to be on the order of 10^7 cm^{-2} using etch-pit density (EPD) approach. Micro-Raman spectroscopy revealed a uniform distribution of residual tensile strain in the as-grown Ge film on Si substrate, which was attributed to the difference in the thermal expansion coefficient between Ge and Si during cooling.

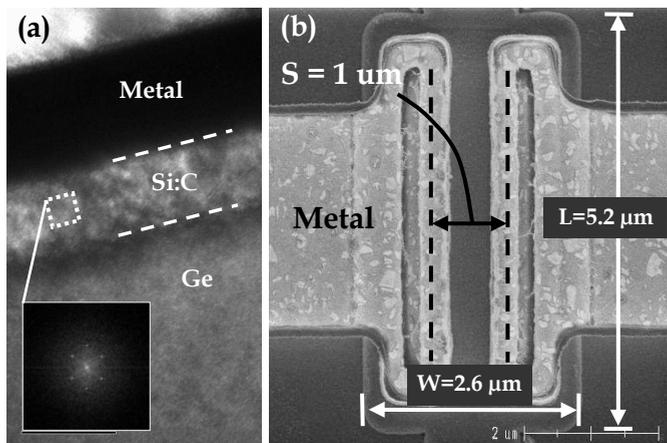


Fig. 12. (a) Silicon-carbon (Si:C) film is bi-dimensional and appears to be of good crystalline quality despite a substantial lattice mismatch between the Si:C barrier and the Ge epitaxial film. (b) SEM image of an evanescent coupled Ge-on-SOI MSM photodetector with an integrated Si micro-waveguide. The Ge detector features an effective device width W and length L of $2.6\mu\text{m}$ and $5.2\mu\text{m}$, respectively. The metal contacts spacing S is $\sim 1\mu\text{m}$.

After contact hole patterning, a thin crystalline silicon-carbon (Si:C) epilayer of ~18nm was selectively deposited in the contact regions using disilane (Si₂H₆) and diluted monomethylsilane (SiH₃CH₃) precursor gases. Such an optimum Si:C thickness was chosen based on the considerations for acting as a good barrier layer to suppress leakage current while achieving low defects density at the heterojunction. Chlorine (Cl₂) precursor gas was intermittently introduced to achieve selective epitaxial growth. The mole fraction of substitutional carbon incorporated in the Si:C film was measured to be ~1% based on the reciprocal lattice vector parameters obtained in X-Ray diffraction (Ang et al., 2007). Meanwhile, the total carbon concentration as obtained from SIMS analysis was found to be equal to ~1.3%, which means that around 0.3% of carbon was incorporated in the interstitial sites. Despite a substantial lattice mismatch, the Si:C layer is bi-dimensional and appears to be of good crystalline quality, as confirmed by the fast Fourier transform (FFT) diffractogram in Fig. 12(a). For comparison, Si:C epilayer was not deposited in a control sample. Metallization consisting of TaN/Al (250Å/6000Å) were subsequently deposited and patterned to complete the device fabrication. Fig. 12(b) shows the scanning electron microscopy (SEM) image of the evanescent coupled Ge-on-SOI MSM photodetector with an integrated Si micro-waveguide. The detector features an effective device length *L* and width *W* of 2.6 μm and 5.2 μm, respectively. The spacing *S* between the metal electrodes of the photodetector was lithographically defined to be ~1 μm.

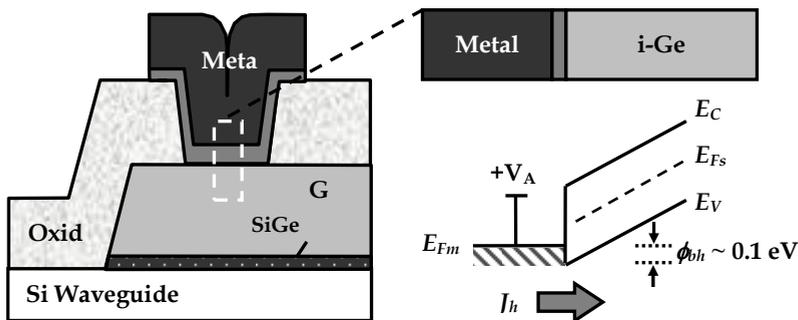


Fig. 13. Cross-sectional schematic of Ge photodetector featuring metal-semiconductor-metal configuration. Strong Fermi level pinning results in a low hole Schottky barrier height, which forms the root cause for the generation of high leakage current.

Fig. 13 depicts the cross-sectional schematic of a MSM configured Ge photodetector structure. Each photodetector can be represented by two back-to-back Schottky diodes. In the absence of the image force lowering effect, the Ge detection region between the metal electrodes will be totally depleted under high applied bias. The total dark current *J_{Total}* flowing through the photodetector can then be described by the following expression

$$J_{Total} = J_p + J_n = A_p^* T^2 e^{-q\phi_{bh}/kT} + A_n^* T^2 e^{-q\phi_{be}/kT} \tag{13}$$

where *J_p* (*J_n*) is the hole (electron) current injected from the anode (cathode), and *A_p^{*}* (*A_n^{*}*) is the Richardson’s constant for hole (electron). Both the hole current and electron current are

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