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GaN-based metal-oxide-semiconductor devices

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1. Introduction

Si-based semiconductors-related technologies are well developed for their applications in electronic devices and integrated circuits (ICs). However, the properties of Si-based semiconductors are seldom being applied in high-frequency and high-power systems. In comparison, the GaN-based semiconductors have also aroused huge interests in recent years owing to their advantages, such as wide and direct energy bandgap, better thermal and chemical stability, and high-electron drift velocity. Therefore, GaN-based semiconductors are widely utilized in electronic devices, including field-effect transistors (FETs) (Khan et al., 1993; Zolper et al., 1996; Klein et al., 1999; Yoshida & Suzuki, 1999; Johnson et al., 2000; Zhang et al., 2000; Jiménez et al., 2002; Binari et al., 2002; Braga et al., 2004; Wallis et al., 2005; Horio et al., 2005; Hong & Kim, 2006; Saripalli et al., 2007) and high-electron mobility transistors (HEMTs) (Egawa et al., 2000; Karmalkar & Mishra, 2001; Vetury et al., 2001; Islam et al., 2002; Koley et al., 2003; Khan et al., 2003; Mizutani et al., 2003; Lu et al., 2003; Meneghesso et al., 2004; Fareed et al., 2005; Inoue et al., 2005; Seo et al., 2008). Among the devices mentioned above, GaN-based HEMTs possess high electron mobility larger than 1000cm²/Vs at room temperature and large operating current due to the formation of two dimensional electron gases (2DEGs). In addition, the GaN-based optoelectronic devices, such as light-emitting diodes (LEDs) (Han et al., 1998; Chang et al., 2004; Fujii et al., 2004; Wierer et al., 2004; Shen et al., 2006; Lee et al., 2006; Chang et al., 2006; Lee et al., 2007; Chen et al., 2007; Chuang et al., 2007), photodetectors (PDs) (Kuksenkov et al., 1998; Walker et al., 1998; Katz et al., 2001; Rumyantsev et al., 2001; Sheu et al., 2002; Seo et al., 2002; Pau et al., 2004; Su et al., 2005; Vardi et al., 2006; Navarro et al., 2009), and laser diodes (LDs) (Nakamura et al., 1996; Nakamura et al., 1996; Saitoh et al., 2003; Suski et al., 2004; Schoedl et al., 2005; Peng et al., 2006; Laino et al., 2007; Braun et al., 2008; Rossetti et al., 2008), have also been investigated and developed extensively for display, lighting, memory system, and communication system in recent years.

It has been reported that utilizing Schottky contact gate could substantially improve the performances of GaN-based metal-semiconductor field-effect transistors (MES-FETs) and metal-semiconductor high-electron mobility transistors (MES-HEMTs) in high-frequency applications (Chumbes et al., 2001; Ohno et al., 2001; Javorka et al., 2002; Okita et al., 2003; Endoh et al., 2004). However, these devices are not suitable for high-power applications because of large gate leakage current, small gate voltage swing (GVS) and small breakdown

voltage. To conquer these aforementioned drawbacks, GaN-based metal-oxide-semiconductor field-effect transistors (MOS-FETs) and metal-oxide-semiconductor high-electron mobility transistors (MOS-HEMTs) are proposed by featuring promising structures and their immense potential in high-power and high-frequency applications (Hu et al., 2001; Kao et al., 2005; Simin et al., 2005; Endoh et al., 2006; Higashiwaki et al., 2006). For MOS devices, the gate insulator plays an important role, since the good quality dielectric layers would yield these devices with outstanding performances. Up to now, several dielectrics, such as SiO_2, Pr_2O_3, Si_3N_4, AlN, Ta_2O_5, MgO, $Ga_2O_3(Gd_2O_3)$, Sc_2O_3, Al_2O_3, and stack dielectric materials, etc. (Arulkumaran et al., 1998; Ren et al., 1999; Hong et al., 2000; Therrien et al., 2000; Rumyantsev et al., 2000; Gaffey et al., 2001; Chen et al., 2001; Lay et al., 2001; Kim et al., 2001; Cho et al., 2003; Ma et al., 2003; Mehandru et al., 2003; Bas & Lucovsky, 2004; Irokawa et al., 2004; Cico et al., 2007) have been used in GaN-based MOS devices and the corresponding electrical characteristics have also been reported. In this chapter, after presenting a brief introduction of the working principle of MOS devices, various dielectric film deposition methods are summarized with a particular emphasis in the photoelectrochemical (PEC) oxidation method. At the same time, the different performances of GaN-based MOS-HEMTs with different insulators are also compared and discussed.

2. Operation principle of metal-oxide-semiconductor devices

2.1 The metal-oxide-semiconductor (MOS) diodes

The metal-oxide-semiconductor (MOS) diodes are key parts of MOS transistors. Fig. 1 shows the cross-sectional schematic configuration of conventional MOS diodes. An oxide film as the insulator layer was deposited on the surface of a semiconductor and then the gate electrode was deposited thereafter on the surface of the oxide film. An ohmic metal contact was formed at the bottom surface of the semiconductor.

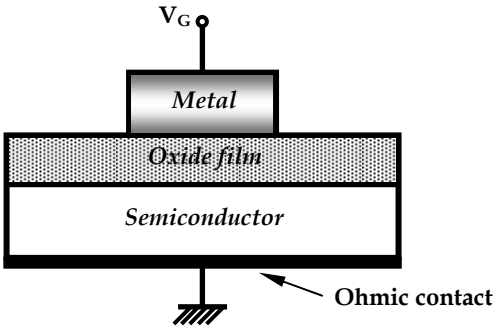


Fig. 1. The cross-sectional schematic configuration of conventional MOS diodes.

Three typical situations are normally occurred at the semiconductor surface, including accumulation, depletion, and inversion, depending on the applied bias between the two electrodes. Fig. 2 shows the energy band diagrams of an ideal MOS diode with n-type semiconductor at different operating conditions (Neaman, 1997). When a positive voltage is applied on the gate electrode of the MOS diode, the free electrons in conduction band of the semiconductor are driven towards the oxide/semiconductor interface, where electrons are accumulated. Accordingly, the energy band at the semiconductor surface is bent downward and

the conduction band edge becomes closer to Fermi level. This is so-called accumulation case, as shown in Fig. 2 (a). When a small negative voltage is applied, the electrons are driven away from the oxide/semiconductor interface by the surface electric field which results in the formation of a depletion region. This case is called depletion case, as shown in Fig. 2 (b). When a larger negative bias is applied, a large number of minority carriers (hole) were induced at oxide/semiconductor interface. Therefore, the energy bands bent upward even more so that the intrinsic level at the surface crosses over the Fermi level. The number of holes (minority carriers) at the semiconductor surface is larger than the number of electron (majority carriers), and in which case it is called inversion and shown in Fig. 2 (c). However, the situation is different for GaN-based MOS diodes, within which the inversion layer is hard to form because the GaN-based material is a wide energy gap semiconductor. The reported results showed that the generation rate of the minority carriers (holes) is extremely low at room temperature (Casey et al., 1996; Hashizume et al., 2000). For an n-type GaN-based material with a carriers concentration of $1.2\times10^{17}cm^{-3}$, the generation time of minority carriers is $t \cong 4.2\times10^{18}s$. However, it is impossible to form an inversion layer with an extremely long generation time. When a negative bias is applied, there are an insufficient number of minority carriers present at the interface and the depletion region extends into GaN to maintain electric neutrality. Consequently, the n-type GaN-based MOS diodes show a deep depletion characteristic at negative bias.

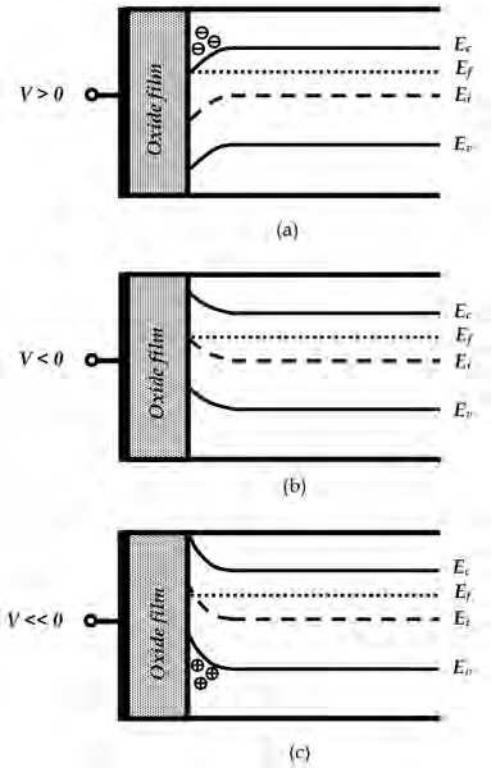


Fig. 2. The energy band diagrams of ideal MOS diode at different operating conditions: (a) accumulation, (b) depletion, and (c) inversion.

2.2 GaN-based metal-oxide-semiconductor field-effect transistors

The GaN-based metal-oxide-semiconductor field-effect transistors (MOS-FETs) is a device which consists of two ohmic electrodes and a MOS diode. Those two ohimc electrodes, located at the two sides of the gate electrode, are connected to GaN-based semiconductor through doped regions. One of the contacts is called the source as it implies that the charge carriers entering the channel originate from this contact, while the other is the drain where the carriers leave the channel. The conductance of the semiconductor near the interface under the gate electrode can be modulated by applying gate bias, as mentioned above for the MOS diode. By applying gate bias, one can modify the effective channel thickness by varying the width of the depletion region, and this in turn varies the output current. If a negative gate voltage is applied on n-channel, the carriers are then depleted from the channel, causing a decrease of the channel conductance; in this case the device behaves as a normally-on (depletion) GaN-based MOS-FETs.

Figure 3 (a) and (b) show the cross-sectional schematic configuration of an n-channel depletion GaN-based MOS-FETs and MES-FETs, respectively. The prior one has better electrical performances due to small gate leakage current, large gate voltage swing and high breakdown field than those of the later one. Fig. 4 shows the depletion layer and the output characteristics of MOS-FETs under various bias conditions (Sze, 2002). As shown in Fig. 4 (a), when gate voltage is zero and drain voltage is small, a small drain current flows from drain to source in the channel and varies linearly with the drain voltage. When the drain voltage increases, the width of depletion layer extends while the cross-sectional area of channel reduces. If the drain voltage is further increased, the depletion layer touches the semi-insulating substrate and the channel became pinch-off, as shown in Fig. 4 (b). The corresponding value of the drain voltage and drain current are called saturation voltage and saturation current, respectively. In Fig. 4 (b), the location P is called the pinch-off point. If the drain voltage increases further, the depletion region widens and pinch-off point then shifts toward the source, as shown in Fig. 4 (c). As the voltage at point P equals to saturation voltage, the current flow in the channel remains fixed. When the drain voltage is larger than the saturation voltage, the drain current becomes independent of the drain voltage. In addition, when a negative voltage is applied to the gate electrode, the electrons are driven away from semiconductor surface, which reduces the electron concentration and forms the depletion layer. Consequently, as the effective channel thickness decreases, and the drain current becomes lower. When the negative gate voltage increases over a certain value, the depletion layer touches the semi-insulating substrate and the channel then operates in a cut-off mode, as shown in Fig. 4 (d). Consequently, the depletion of n-channel depletion-mode MOS-FETs at semiconductor surface can be achieved by applying a sufficient gate bias to inhibit the device current. The GaN-based MES-FETs have similar behaviors. When Schottky gate metal contacts to semiconductors as shown in Fig. 3 (b), the depletion region forms at the metal/semiconductor interface and its width can be controlled by gate bias as mentioned above.

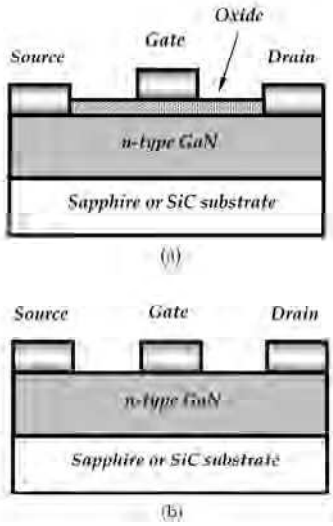


Fig. 3. The cross-sectional schematic of an n-channel depletion (a) MOS-FETs and (b) MES-FETs.

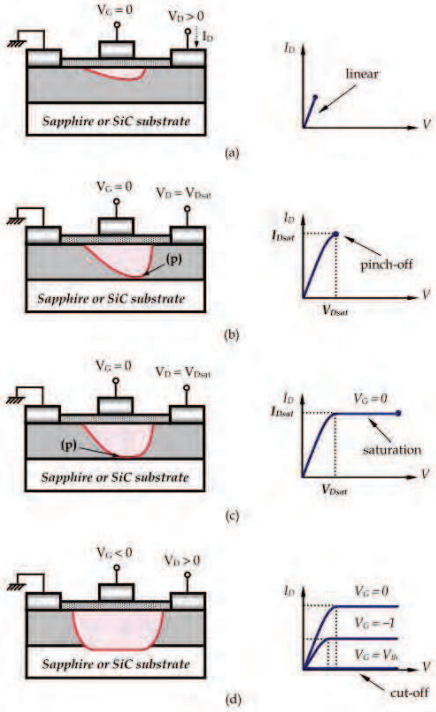


Fig. 4. The depletion layer width and output characteristic of MOS-FETs at various bias conditions. (a) V_G=0 and a small V_D voltage (b) V_G=0 and at pinch-off (c) V_G=0 and at post pinch-off (V_D>V_{Dsat}) (d) a negative V_G voltage and at cut-off case.

2.3 GaN-based metal-oxide-semiconductor high-electron mobility transistors

Metal-oxide-semiconductor high-electron mobility transistors (MOS-HEMTs), namely metal-oxide-semiconductor heterojunction field-effect transistors (MOS-HFETs) (Sze, 2002), are another kind of field effect transistor, which is similar to the MOS-FETs but with its semiconductor layer replaced by a semiconductor heterostructure. Figure 5 shows the energy band diagram of the AlGaN/GaN heterostructure. The band gap of AlGaN (low electron affinity) is wider than the bandgap of GaN (high electron affinity). When they form junctions, both the conduction band and valence band at the AlGaN/GaN interface bend and the conduction band of GaN drops below the Fermi level. Consequently, a triangular potential well is formed at the GaN side of the interface, owing to the conduction band discontinuity. The electrons are confined in this well, and forming a two dimensional electron gas (2DEG). In addition, the spontaneous polarization (Ambacher et al., 1999; Ambacher et al., 2000) and piezoelectric polarization (Smorchkova et al., 1999; Sacconi et al., 2001) effects, which are large in the wurtzite GaN-based semiconductor materials (Johnson et al., 2001; Lu et al., 2001), provide a further improvement in the sheet carrier concentration of the 2DEG, which is typically up to $10^{13}cm^{-2}$. Furthermore, the 2DEG are located in the region of the undoped GaN, where the carrier mobility is high as the scattering effect is reduced.

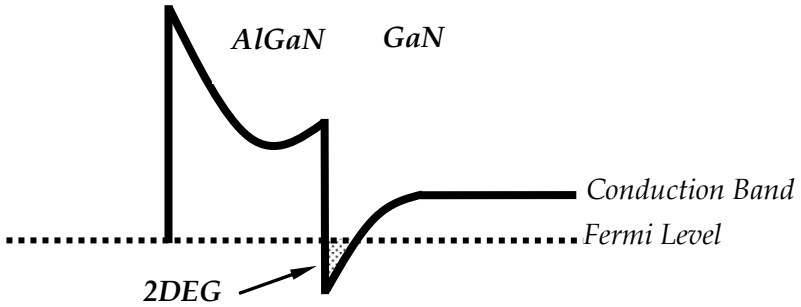


Fig. 5. The energy bandgap diagram of AlGaN/GaN heterostructure.

Figure 6 (a) and (b) shows the schematic configuration of AlGaN/GaN MOS-HEMTs and MES-HEMTs grown on sapphire substrates (Al_2O_3) using metalorganic chemical vapor deposition (MOCVD) system or molecular-beam epitaxy (MBE) system. The carbon-doped GaN layer has high resistance and can confine the carriers transport in the AlGaN/GaN channel (Webb et al., 2001). The electrons transport occurs in the 2DEG channel between two ohmic contacts of source and drain electrode. The insulators are deposited in the drain-source region for surface passivation and gate insulation. The source is usually grounded and the voltage applied between the drain and source is called V_{DS}, while the gate-source voltage is called V_{GS}. The current flowing from source to drain is called I_{DS} and I_{GS} is the current entering the gate through the oxide film. This is the reason why the MOS-HEMTs have small gate leakage current and large breakdown voltage compared to those of MES-HEMTs. The ability of the gate electrode to modulate the source-drain current is expressed as the extrinsic transconductance $g_m=\partial I_{DS}/\partial V_{GS}$. The conductance of the channel varies with the sheet carrier concentration, which is modulated by the gate bias. When the gate bias is positive, more electrons accumulate in the 2DEG channel and the operation current of

AlGaN/GaN MES-HEMTs will be larger. The current decreases with the decrease of the gate bias. The 2DEG channel will be fully depleted and the drain-source current will drop to zero when the gate bias reaches a negative threshold value, which is called cut-off voltage or threshold voltage. This corresponds to the case of which the MOS-HEMTs operating in the depletion mode.

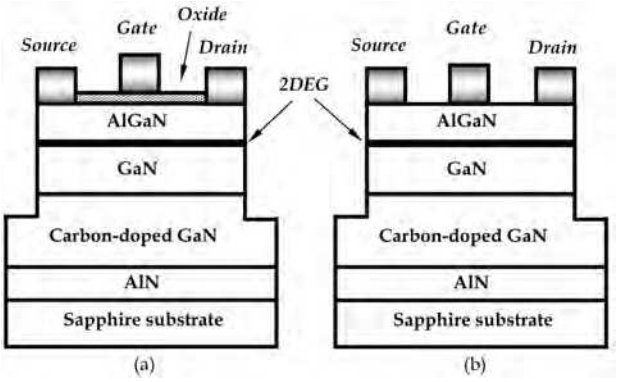


Fig. 6. The schematic configuration of AlGaN/GaN (a) MOS-HEMTs and (b) MES-HEMTs.

3. Obstacle to further improving transistor performances

For GaN-based MES-HEMTs and MOS-HEMTs, there are still some problems to be solved, which limit their performances ultimately. Among them, the self-heating (Gaska et al., 1997; Gaska et al., 1998; Ahmad et al., 2006) and current collapse (Klein et al., 2001; Mittereder et al., 2003; Kuzmik et al., 2004; Zheng et al., 2008) are the most serious effects that degrade the high-frequency and high-power performances of the transistors.

The self-heating effect occurs usually when the transistor operates at high drain-source voltage. Fig. 7 gives a typical example where the drain current decreases at high DC drain-source voltage (Fan et al., 2004). This is related to the fact that the electrons flowing in the device transfer part of their energy to the lattice via trap-related scattering and electron-phonon interaction (Bhapkar et al., 1997), which raises the channel temperature of the devices. This effect is induced by the poor thermal conductivity of the sapphire substrates which are commonly used for fabricating GaN-based transistors. The self-heating effect can be suppressed by using highly thermal conductive SiC substrates in stead of sapphire substrates (Morkoc et al., 1994).

During epitaxial processes, traps exist in GaN buffer layer, AlGaN layer and AlGaN surface. Traps on the semiconductor surface capture electrons and form lots of virtual gates. Those virtual gates deplete the channel and make the drain-source current is smaller than ideal value. In addition, when high drain-source electrical field is applied, some hot electrons transfer from 2DEG channel to adjacent layer with high concentration of traps. Those factors cause the drain-source current decrease and this phenomenon is called the current collapse. The simple schematic configuration of current collapse of transistors is shown in Fig. 8 (Zheng et al., 2008). It can be suppressed by surface passivation and gate insulation by depositing dielectrics on AlGaN surface (Tan et al., 2002; Arulkumaran et al., 2004) or using

confinement layer underlying 2DEG channel (Palacios et al., 2006). For obtaining better radio-frequency (rf) performances and power performances, suppressing those two unideal effects is urgent.

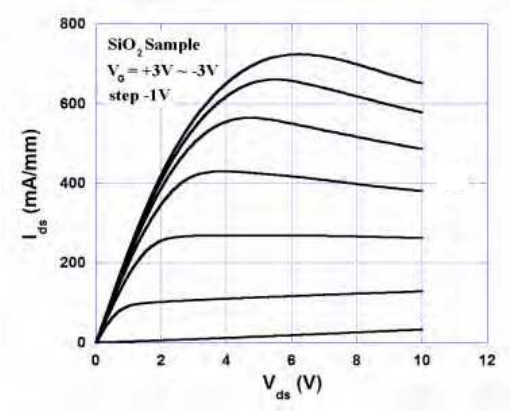


Fig. 7. Self-heating in an AlGaN/GaN MOS-HEMT.

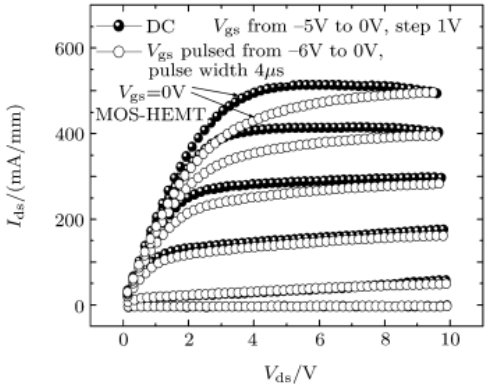


Fig. 8. Current collapse in an Al_2O_3/AlGaN/GaN MOS-HEMT (dashed lines: Before stress; solid lines: After stress).

In addition, the low frequency noises, such as flicker noise, and generation-recombination noise, mean the inevitable disturbances of output signals when devices operated at a low frequency. Fig. 9 shows the spectra of flicker noise and generation-recombination noise. The prior one is proportional to inverse frequency but the later one has Lorentizn distribution. Flicker noise is an important indicator for judging the transistors weather they are suitable for communicating applications or not, because a large level of flicker noise limits the phase noise characteristics and causes the performance degradation of the electronic systems (Balandin et al., 1999). The interface-state densities, defects, and phonons are possible sources of flicker noise. Furthermore, it is a useful tool for confirming crystal quality, and manufacture techniques (Balandin et al., 1999; Balandin et al., 2000). In general, MOS-HEMTs have better behavior in flicker noise than MES-

HEMTs, because the interface-state densities in MOS-HEMTs are well passivated (Vertiatchikh & Eastman, 2003; Chiu et al., 2008). Fabricating transistors with low flicker noise is a vital issue for developing high performance electronic devices and systems.

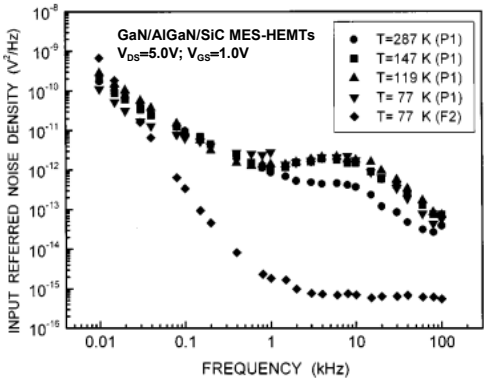


Fig. 9. Low temperature noise characteristics of the GaN MES-HEMTs in the subsaturation regime. Generation-recombination (g-r) bulges are clearly seen in spectra of the doped channel device (P1) at frequency f ≈3–4 kHz.

4. Method of growing gate insulators of GaN-based MOS devices

For fabricating GaN-based MOS devices with excellent performances, an important task is, as with the other MOS devices, to find suitable right methods to form a proper insulator layer on the semiconductor. Many efforts have been focused on the exploration of insulator materials and deposition methods. In most of cases reported in the literature, the insulator layers of the GaN-based MOS devices were deposited externally onto the semiconductor surface by physical vapor deposition (PVD) and chemical vapor deposition (CVD) methods. The main results reported in the literatures will be reviewed first. Then, we will give a more detailed discussion on photoelectrochemical (PEC) oxidation method, with which the oxide layer is formed via a chemical reaction with the semiconductors, instead of relying on an external deposition.

4.1 Electron-beam deposition method

The electron beam evaporation employs an electron-beam emitted by a filament of the electron gun to bombard the target in a high vacuum chamber. The kinetic energy of the electron-beam transforms into the thermal energy upon contact of the target, which in turn melts the target. The e-beam evaporation has good thermal translation efficiency and high evaporation rate. In addition, the current can be controlled, so as to judiciously control the evaporation rate. There are basically no limits to which the materials can be evaporated with the electron-beam evaporation method. The materials can easily be evaporated irrespective of their purity and chemical compounds. The target is placed into a crucible with an adequate cooling through proper arrangement. High thermal melt zone is localized around a position of the target which is bombarded directly by an electron-beam.

Several conventional gate oxides such as $Ga_2O_3(Gd_2O_3)$, SiO_2, TiO_2, AlN, MgO, Ta_2O_5, Pr_2O_3 and stack dielectrics have been deposited using e-beam deposition system for gate insulators of GaN-based MOS devices (Hong et al., 2000; Arulkumaran et al., 2005; Kikuta et al., 2006; Yagi et al., 2006; Chiu et al., 2008). Figure 10 shows the typical capacitance-voltage characteristics of GaN MOS diode with $Ga_2O_3(Gd_2O_3)$ as the gate insulator, measured at various frequencies. The capacitance measured at forward bias is originated by capacitance of oxide films. The smaller capacitance at reverse bias is due to the capacitances in series originated from the oxide layer and the depletion region. The frequency dispersion observed in accumulation mode is attributed to the traps existed in the inner oxide layer. This phenomenon is induced from the Maxwell-Wranger effect (Hippel, 1954). The obtained density state (D_{it}) is less than $10^{11}cm^{-2}eV^{-1}$. The ln(J) v.s. V characteristics of the GaN MOS diodes are shown in Fig. 11. It can be seen that the $Ga_2O_3(Gd_2O_3)$ insulator grown using the electron-beam deposition method exhibits good insulation properties.

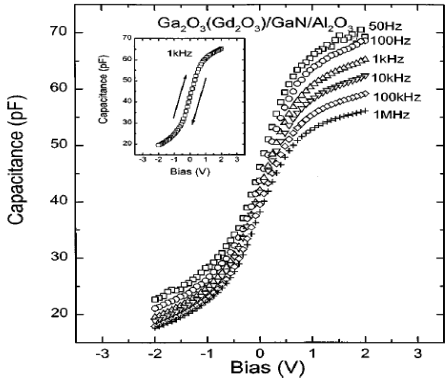


Fig. 10. The capacitance-voltage characteristics of $Ga_2O_3(Gd_2O_3)$/GaN MOS diodes.

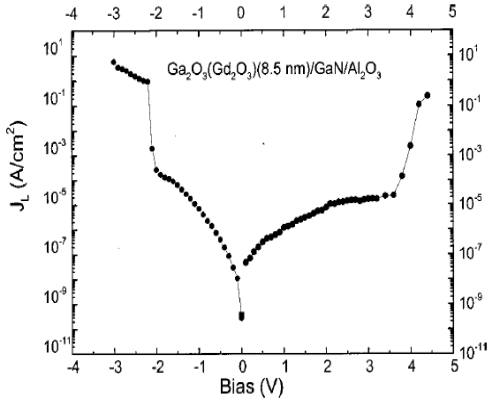


Fig. 11. The current-voltage characteristics of $Ga_2O_3(Gd_2O_3)$/GaN MOS diodes.

The drain-source current-drain-source voltage (I_{DS}-V_{DS}) characteristics of SiO_2/AlGaN/GaN MOS-HEMTs and AlGaN/GaN MES-HEMTs are reported by Arulkumaran and Egawa, et al., and shown in Fig. 12 (a) and (b), respectively (Arulkumaran et al., 2005). It can be seen

that the $I_{DS(max)}$ of MOS-HEMTs is about 856mA/mm which is larger than that of MES-HEMTs. Fig. 13 (a) and (b) show the gate leakage current (I_g) as a function of gate-source voltage and the transfer characteristics of MOS-HEMTs and MES-HEMTs, respectively. At reverse voltage of 40V, the I_g of MOS-HEMTs is about three orders smaller than that of MES-HEMTs The $g_{m(max)}$ of MOS-HEMTs and MES-HEMTs are 160mS/mm and 145mS/mm, respectively. Better direct-current (dc) performance can be obtained with the improvement of the extrinsic transconductance of transistors. These results show that the electrical performance can be enhanced through the surface passivation and gate insulation. The similar behaviors of AlGaN/GaN MOS-HEMTs with different gate insulators can be observed in other reports (Kikuta et al., 2006; Yagi et al., 2006).

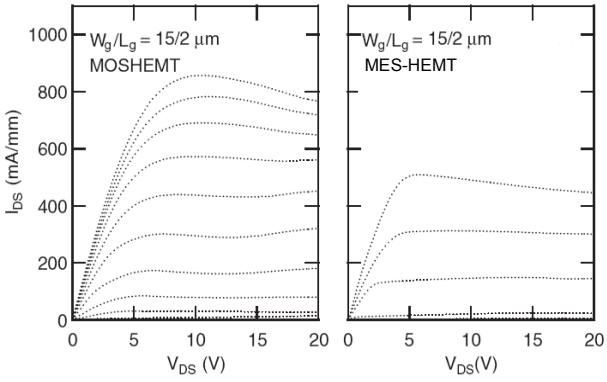


Fig. 12. The I_{DS}-V_{DS} characteristics of (a) SiO_2/AlGaN/GaN MOS-HEMTs and (b) AlGaN/GaN MES-HEMTs.

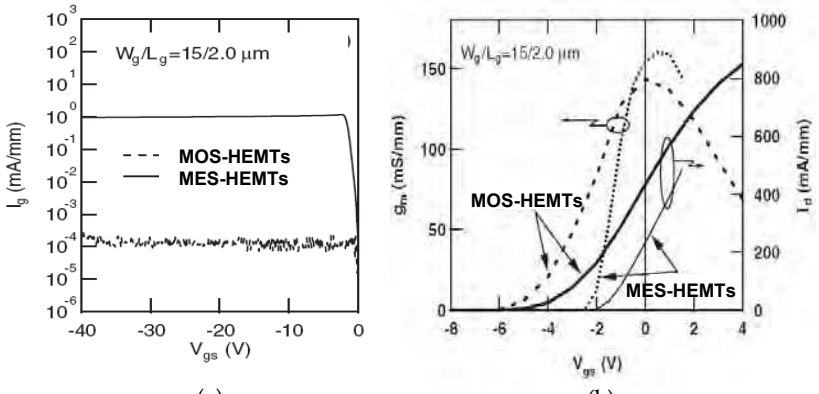


Fig. 13. The dc electric performance of MOS-HEMTs and MES-HEMTs (a) the gate leakage current as a function of gate-source voltage and (b) the transfer characteristics.

Investigating dielectrics with high permittivity is an interesting issue for better high-frequency and high-performances due to the suppression of gate leakage current and

current collapse by applying gate dielectrics in AlGaN/GaN MOS-HEMTs. However, the decrease of the transconductance (Ye et al., 2005) and the large shift of the threshold voltage are obvious expenses. Using dielectrics with high permittivity (high-k) is helpful to solve these problems. A larger dielectric constant could translate to an efficient gate modulation (Liu et al., 2006); thus, a smaller decrease in transconductance and a moderate increase in the threshold voltage could be expected in MOS-HEMTs with high-k gate insulators. The Pr_2O_3 high-k dielectrics (k=30) have also been deposited using an electron-beam evaporator for gate insulation and surface passivation of AlGaN/GaN MOS-HEMTs (Chiu et al., 2008). Fig. 14 shows the flicker noise spectra of MES-HEMTs and MOS-HEMTs, respectively. It can be seen that the level of flicker noise of the MOS-HEMTs is smaller than that of the MES-HEMTs. It means that the lower surface states and gate leakage current is achievable with high-k Pr_2O_3 films grown using an electron-beam evaporator. The microwave-power characteristics of both devices are shown in Fig. 15. The maximum output-power density and PAE are 753mW/mm and 36.8% for MOS-HEMTs at an input power of 15dBm, which are better than those of the MES-HEMTs with corresponding values of 698mW/mm and 32.1%, respectively.

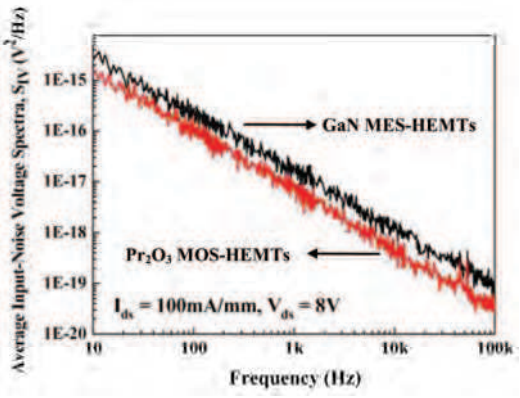


Fig. 14. Flicker noise spectra of MES-HEMTs and MOS-HEMTs, respectively.

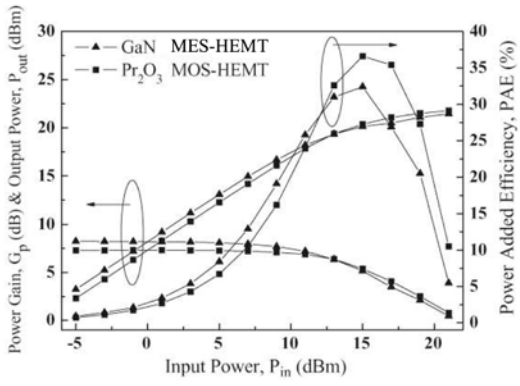
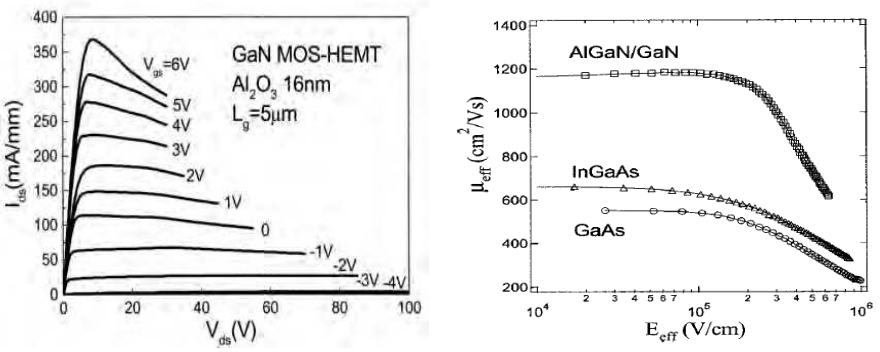


Fig. 15. The mircorwave-power characteristics of MES-HEMTs and MOS-HEMTs.

4.2 Atomic layer deposition (ALD) deposition method

The atomic layer deposition (ALD) deposition is a technique for growing thin films on various substrates with atomic scale precision based on alternate saturated surface reaction in each cycle of deposition. ALD is a chemical gas phase deposition process. The growth of thin film is self-limited and based on surface reaction. The deposition of conformal thin-films onto substrates of varying compositions via sequential surface chemistry enables controllable atomic scale deposition. ALD reaction divides the CVD reaction into two half-reactions. The ALD deposition has several advantages over other techniques, including high quality deposited films, excellent conformity and reproducibility. A variety of thin films can be deposited utilizing ALD deposition with high density and low impurity at a low deposition temperature.

The Al_2O_3 and HfO_2 dielectrics are common insulators grown using ALD system and have been applied in AlGaN/GaN MOS-HEMTs (Park et al., 2004; Ye et al., 2005; Wu et al., 2006; Kim et al., 2007; Medjdoub et al., 2007; Yue et al., 2008; Feng et al., 2009; Chang et al., 2009). The qualities of Al_2O_3 films gauged by several important figures of merit including uniformity, defect density and stoichiometric ratio of the deposited films, are comparably better, when ALD is chosen over the other deposition methods such as sputtering and electron-beam deposition methods. The I_{DS}-V_{DS} and effective electron mobility characteristics of GaN MOS-HEMTs are shown in Fig. 16 (a) and (b), respectively. The $I_{DS(max)}$ of MOS-HEMTs at V_{GS}=6V is 375mA/mm and the off-state breakdown voltage is 145V. In addition, the negative output conductance under high drain bias is due to self-heating effect. The effective carrier mobility (μ_{eff}) of insulator/AlGaN/GaN structure as a function of effective electric field (E_{eff}) is larger compared to the other semiconductors, which implies devices sharing this kind of structure do possess excellent high-frequency and high-power performances.



(a) (b)

Fig. 16. The measured (a) I_{DS}-V_{DS} and (b) effective electron mobility of AlGaN/GaN MOS-HEMTs.

The HfO_2 insulator is a promising candidate because of its high dielectric constant (20~25) and large bandgap (5.6~5.8eV). Al_2O_3 is also a potential candidate for the above application, which has a good passivation effect and low interface state density. The Al_2O_3 is a better insulator for interfacial passivation layer (IPL) application in high-k gate process of

AlGaN/GaN MOS-HEMTs because it has better chemical and thermal stabilities against AlGaN compared to HfO_2 films (Gusev et al., 2006). The HfO_2/Al_2O_3 stack gate dielectrics deposited using ALD system utilized in AlGaN/GaN MOS-HEMTs are reported by Yue and Hao, et al. (Yue et al., 2008). The $g_{m(max)}$ of MES-HEMTs and MOS-HEMTs are 165mS/mm and 150mS/mm, respectively. The decay of the transconductance is due to the increase of the distance between the channel and Schottky gate of the MOS-HEMT structure. Furthermore, the negative shift in threshold voltage from –4V of MES-HEMTs to –5V of MOS-HEMTs is caused by the same reason. The decrease of $g_{m(max)}$ is only 9% and therefore is better compared with the deterioration degree of transconductance in MOS-HEMTs with low-k gate insulators (Kordos et al., 2005). The gate voltage swing (GVS) of MES-HEMTs and MOS-HEMTs are 2.4V and 1.8V, respectively. MOS-HEMTs not only have better linear operation because of large GVS compared to HEMTs, but also have a smaller intermodulation distortion, a smaller phase noise, and a larger dynamic range. These advantages ultimately render them suitable for practical amplifier applications (Khan et al., 2006). The pulse current-voltage performances of Al_2O_3 passivated MES-HEMTs and stack gate MOS-HEMTs are shown in Fig. 17. The current collapse phenomenon ascribed to the interface state density can not be observed in both devices and therefore it is reasonable to assume the surface states are well passivated in both transistors. Moreover, the unity current gain cut-off frequency and the maximum frequency of oscillation are 12GHz and 34GHz, respectively, as depicted in Fig. 18. According to the results mentioned above, the MOS-HEMTs not only have excellent dc and pulse mode electrical performances than those of passivated MES-HEMTs, but also exhibit outstanding high-frequency properties.

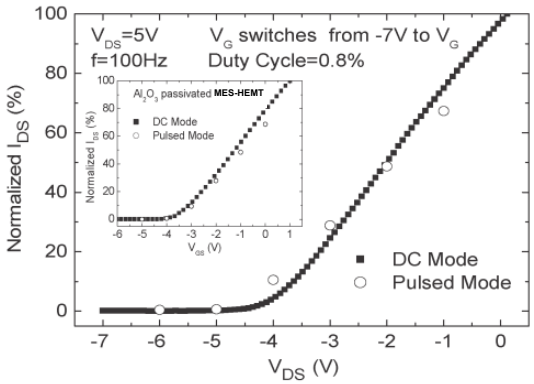


Fig. 17. The pulse current-voltage characteristics of Al_2O_3 passivated MES-HEMTs and stack gate MOS-HEMTs.

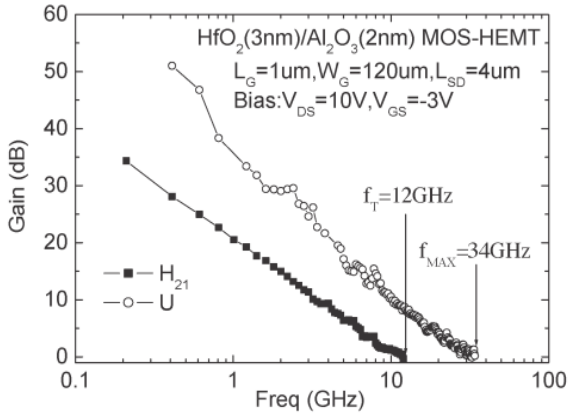


Fig. 18. The short-circuit current gain (H_{21}) and unilateral power gain (U) versus frequency of MOS-HEMTs operated at V_{DS}=10V and V_{GS}=–3V.

4.3 Sputter deposition method

Usually, a sputtering deposition involves two electrical plates in the vacuum chamber and one of them is used to accommodate a target material. When a negative voltage is applied to the target (i.e. cathode) by an external power supply, a number of free electrons are accelerated toward the anode. While on their way to anode these free electrons would expect to hit other gas molecules and then ionize them in the chamber, if the energy of the accelerated electrons is sufficiently high enough. Due to the negative voltage applied on target, the energy of these positive ions attracted toward the target surface depend on the applied voltage. When accelerated positive ions collide with the surface atoms of the target material, their energy are imparted to the target molecules, so that they can be ejected or sputtered out from the surface of the target material. Sputtering of target material is a possible outcome only, when the bombarding ion energy is large enough to disrupt the target molecules. Sometimes the ions bombarding the cathode may knock the electrons out from it, causing them to accelerate under the influence of applied field to enhance a chain of reactions involving the necessary ionization of molecules and the sputtering process. Magnetron sputtering is a powerful and flexible technique and the sputtering process almost places no restriction in the choice of the target materials; these include using a dc power to sputter pure metals and a rf power or pulsed dc power source to sputter semiconductors and isolators.

The performances of GaN-based MOS devices with insulators grown by sputtering technology are demonstrated (Nakano & Kachi, 2003; Liu et al., 2007; Jhin et al., 2008; Shih et al., 2009). Liu and Chor, et al. have reported the performances of AlGaN/GaN MOS-HEMTs with HfO_2 high-k dielectrics deposited using sputtering system (Liu et al., 2006). The I_{DS}-V_{DS} and transfer characteristics are shown in Fig. 19 (a) and (b), respectively. The $I_{DS(max)}$ of 830mA/mm is obtained at V_{DS}=6V. In addition, the self-heating effect does not be found under the high drain-source current operation, because the Si substrate has better thermal conductivity. The GVS and $g_{m(max)}$ of MOS-HEMTs are 2.91V and 115mS/mm, respectively. The negative shift in threshold voltage from –4V of MES-HEMTs to –6V of MOS-HEMTs is

caused by the increase in distance between gate and channel. Figure 20 shows the dc and pulse mode measurement of MES-HEMT and MOS-HEMT respectively. The V_{DS} bias is held at 8V and the frequency of pulsed V_{GS} is 100kHz. There is 60% drain current discrepancy between the dc and pulsed modes associated with MES-HEMTs. However, a significant drain current recovery is observed in MOS-HEMTs. This phenomenon clearly indicates that the HfO_2 layer can passivate the traps on AlGaN surface that otherwise would create a depletion region and suppress the current collapse.

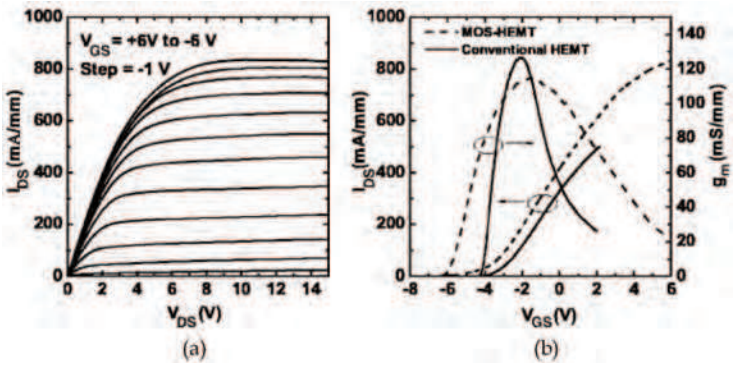


Fig. 19. The (a) I_{DS}-V_{DS} of MOS-HEMTs and (b) transfer characteristics of MES-HEMTs and MOS-HEMTs.

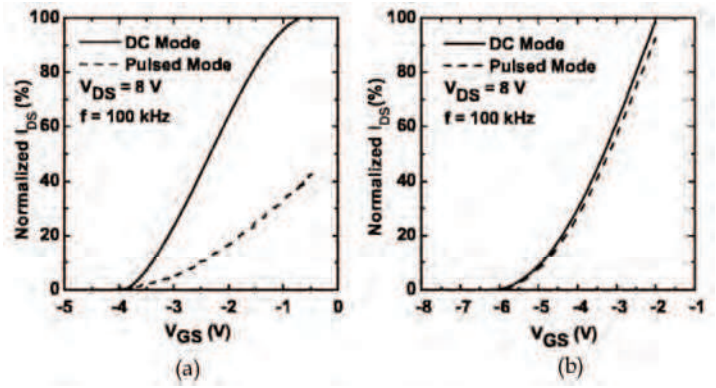
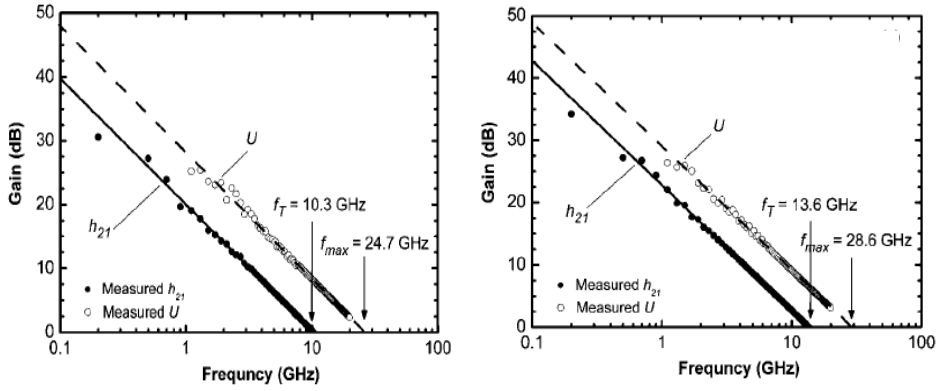


Fig. 20. The dc and pulse mode measurement of AlGaN/GaN (a) MES-HEMTs and (b) MOS-HEMTs.

The relationship between gate insulation and high-frequency performances are also investigated (Liu et al., 2007). The high-frequency performances of AlGaN/GaN HEMTs with and without HfO_2 gate insulator are shown in Fig. 21 (a) and (b), respectively. The improvement of f_T and f_{max} is attributed to the increase of transconductance.



(a) (b)

Fig. 21. The S-parameter measurement of AlGaN/GaN (a) MES-HEMTs and (b) MOS-HEMTs.

4.4 Jet vapor deposition (JVD) method

The jet vapor deposition (JVD) is a novel process for synthesizing wide variety of thin films of metals, semiconductors, and insulators (Ma, 1998). It relies on supersonic jets of a light carrier gas such as helium to transport depositing vapor from the source to the substrate. Because of the separation of the constituent depositing species, and their short transit times, there is very little chance for gas-phase nucleation. In contrast to the conventional CVD silicon nitride, the high-field I-V characteristics of the JVD silicon nitride fit the Fowler-Nordheim (F-N) tunneling theory over 4-5 orders of magnitude in current, but do not fit at all with the Frenkel-Poole (F-P) transport theory. This is consistent with a much lower concentration of electronic traps in the JVD silicon nitride.

The JVD is a novel and interesting technology. The $SiO_2/Si_3N_4/SiO_2$ stack gate insulators of GaN MOS devices grown using JVD system were reported (Gaffey et al., 2001; Ma et al., 2003). Figure 22 (a) shows the measured and theoretical capacitance-voltage characteristics performed at a room temperature and a frequency of 10kHz. The open circle and solid line indicate the measured data and theoretic value of capacitance-voltage (C-V) characteristics, respectively. It can be seen that the measured data are fitted well to theoretic data with out any translation along the voltage axis. This phenomenon indicates that the net density of fixed charges within the insulator is very low. Fig. 22 (b) shows the C-V performances at different frequency at 450°C. The near ideal curve means that the devices work well up to 450°C. The interface-state density (D_{it}) of devices should be low because of weak frequency dependence. The inset shows a magnified view of this C-V curve with respect to a particular voltage region and note that the small frequency dependence is observed.