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Continuous-Time Analog Filtering: Design Strategies and Programmability in CMOS Technologies for VHF Applications

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1. Introduction

The evolution of wireless applications (the performance as well as the number of users) has undergone explosive growth in the last years, resulting in an increasing demand for smaller, low-cost wireless transceivers with low power consumption. In order to meet this demand, continuous development must take place both in CMOS technology and in RF electronics, the goal of which should be to achieve a fully-integrated single-chip receiver in a low-cost CMOS process. This demand for complex read channel and multi-standard receiver ICs calls for the design and implementation of one category of analog interface chips as continuous-time (CT) filters, suitable for high speed with variable bandwidths over a wide frequency range, preferably using the G_m-C approach rather than other existing solutions.
Filters based on the G_m-C technique were used quite early on with bipolar technology and they have now become the dominant option to implement monolithic filters for very high frequency. The basic building block of a G_m-C filter is the integrator, which involves the use of transconductors and capacitors only and whose structure is therefore simpler than others, such as operational amplifiers. The simplicity of the transconductor coupled with the open-loop operation, which does not involve any complex frequency compensation schemes, point to this cell as the basic active element to be considered and the best option to operate in a VHF range with low supply voltages.

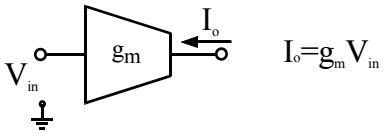

Fig. 1. Ideal transconductor V_{in} to I_o converter of transconductance g_m (conversion factor).

All the benefits of the G_m-C approach lie in the ideal behaviour of the transconductor. Nevertheless, its use as the basic element in the VHF active filter implementation forces one to consider some drawbacks related with the non-idealities of this fundamental cell: finite output resistance, finite bandwidth, noise, non-linearity, etc. The main disadvantages inherent to this technique are its high sensitivity to parasitic capacitors and the non-linear

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behaviour of the transconductor, to the extent of appearing a distortion brought about mainly by the non-linearities generated in the V-I conversion. Certain specific strategies require to be used to minimize these effects.

By taking differential or balanced transconductor structures into account, distortion is reduced (even non-linear components are cancelled) and better immunity to common-mode noise is obtained. Furthermore, the use of tuning techniques compensates parameter deviations due to process and temperature variations. These ideas, together with a careful layout, a detailed study of the technology and a deep analysis of the device, lead to an improvement in the transconductor behaviour, and consequently, in the filter performance. Thus, while developing the design of an active G_m-C filter, the effects of transconductor non-idealities must be analysed in depth to achieve optimum filter performance. The implementation of the transconductor should show a trade-off between dc-gain, linearity and low phase-error at the cut-off frequency.

Any pole or zero frequency in filters based on the G_m-C technique is of the G_m/C type. This means that there are two fundamental ways of programming the frequency response of the filter: keeping G_m constant and varying C, or vice versa. The choice of filter approach will affect noise and power dissipation (Pavan et al., 2000). The constant-C approach has the advantage of maintaining the noise specifications constant over the entire programming range while decreasing the power consumption for lower frequencies. Due to the above considerations, the constant-C scaling technique is the preferred approach for implementing filters operating in a very high frequency range, focusing on the design of tunable CMOS transconductors. On the other hand, discrete tuning is currently being more widely used than continuous tuning, both to preserve the dynamic range and take advantage of the digital system in mixed design to determine the control signal that calibrates and reconfigures the filter. A possible discrete tuning technique is based on a parallel connection of transconductors, where the desired time-constant can be digitally programmed (Pavan et al., 2000a). This approach succeeds in keeping the Q-factor constant and maintains an adequate dynamic range over the entire bandwidth setting.

The target is to implement a transconductor that is compatible with the latest low-cost pure digital CMOS technologies and programmable over a very high frequency range while maintaining an adequate dynamic range (DR). The concrete values of these specifications depend on each particular application. This work does not focus on a concrete application but on carrying out an overall analysis to seek the structure that provides the best trade-off between operation frequency, programmability, dynamic range and power consumption.

Considering all these points, an optimal solution for digitally programmable analog filters in the VHF/UHF range is to take advantage of current-mode pseudo-differential topologies and endow them with digital programmability. The design strategy is therefore as follows: after analysing the transconductor parameters that limit its ideal behaviour, a very well-known current-mode topology (Smith et al., 1996; Zele et al., 1996) will be characterized; starting from the Zele-Smith architecture, two different transconductors will be presented and in-depth analysis will be carried out, following which all the characteristic parameters of each active cell will be obtained; programmability will then be added to the VHF transconductors and the experimental results of a low-cost 0.35 μm CMOS implementation will be presented. As the active cell is based on a classical structure, a broad diversity of digitally programmable and continuously tunable CT filters can be obtained, where the programmability exhibited by the filter is achieved due to the design of a generic programmable transconductor. Due to the lack of special capacitor structures in standard digital technologies, the use of the MOS structure as

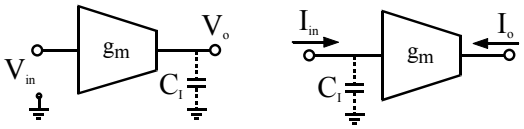
an intended passive device is probably as old as the MOS transistor concept itself. An alternative to implementing linear capacitors is to use the *gate-to-channel capacitance* of MOSFET devices as capacitors, where the gate-oxide thickness is a well-controlled variable in the process. This option will be considered in this work.
Therefore, in this chapter we will show the best way to implement key analog building blocks of a high-speed system in a CMOS technology with a wide programmable frequency range; considering new design techniques and uncovering potential problems associated with the design of high-speed analog circuits using short-channel and low-voltage devices. These are the challenges of CMOS filter design at very high frequencies and this study addresses the theoretical and practical problems encountered in the design of robust, programmable continuous-time filters with very high bandwidths implemented in low-cost digital CMOS technologies.

2. The Integrator: building-block in the Gm-C technique

The majority of continuous-time (CT) integrated filters, circuits where high frequency at low cost of silicon and power is required, present a frequency response controlled by time-constants, and one of the simplest implementations for these factors is taking advantage of the integrator structure. Therefore, the integrator is the dominant building block for many high-frequency active circuit design techniques, and its frequency response and linearity directly determine the filter performance.
Accordingly, systems based on the G_m-C technique are the first option for implementing CT filters, thanks to their acceptable performance over the VHF range. The active building element used by the G_m-C filter approach, based on an open-loop integrator, is the transconductor cell (Fig. 1), which ideally delivers an output current proportional to the input signal voltage:

$$I_o = g_m V_{in} \tag{1}$$

where g_m is the transconductance of the element. When a grounded capacitor is connected to the output node of the transconductor in order to take this current out, an integrator is obtained leading to V_{in}-V_o conversion, as shown in Fig. 2(a). It turns out that an ideal voltage-mode integrator has been obtained with a simple transconductance-capacitor combination. Nevertheless, a second structure can be considered taking into account the current-mode signal processing, whereby two different, yet completely equivalent, topologies are obtained. In this case, the input current is taken across the integration capacitance in order to obtain the transconductor input voltage and then, after the active cell, the output current. Thus, Fig. 2(b) shows the I_{in}-I_o conversion.



(a) (b)

Fig. 2. Ideal integrator; (a) voltage-mode: $\frac{V_o}{V_{in}} = -\frac{g_m}{sC_1}$, (b) current-mode: $\frac{I_o}{I_{in}} = \frac{g_m}{sC_1}$.

Due to the grounded location of most parasitic capacitors of the active cell (the total output/input node effective parasitic capacitance, depending on the configuration), they must be considered by constituting a percentage of the total integration capacitance C_I, which is particularly significant at high frequencies. An extreme situation can be reached when considering the proposed transconductor as an integrator where total integration capacitance C_I is constituted only by these parasitic capacitances, with no need for any external capacitor. Nevertheless, these capacitances are not linear and, depending on their contribution, the total linearity of the system will be affected. As technological process variations will also affect the value of these parasitic capacitances, sensitivity to these capacitors requires a detailed study of the device models and integration technology together with a careful system layout.

The ideal integrator has an infinite dc-gain and no parasitic effects, thus obtaining a phase of $-\pi/2$ for all the frequencies. The unity-gain frequency is $\omega_t=g_m/C_I$. Nevertheless, a real integrator presents a non-zero transconductor output conductance g_{out} and parasitic poles and zeros, which distort the transfer function:

$$H(s) = A_{DC}\frac{\left(1-{}^{s}\!/_{\omega_2}\right)}{\left(1+{}^{s}\!/_{\omega_1}\right)} \tag{2}$$

where $A_{DC}=g_m/g_{out}$ is the dc-gain and $\omega_1=\omega_t/A_{DC}=g_{out}/C_I$ is the frequency of the dominant pole. The effects of parasitic poles and zeros at frequencies much higher than the frequency range of the transconductor can be modelled with a single effective zero ω_2: positive ω_2 results in an effective parasitic RHP-zero and negative ω_2 in an LHP-zero.

Non-zero transconductor output conductance g_{out} causes finite dc-gain in real integrators in the filter. In addition, parasitic poles and zeros in the integrator transfer function, together with finite A_{DC}, generate deviations of the inverter integrator phase response from $-\pi/2$, and it is well-known that phase error is the main source of misfunctions in filters. In particular, phase deviations around ω_t can cause significant errors in the filter transfer, depending on filter quality factors. The accuracy of the overall frequency response of the filter depends on how closely the individual integrators in the filter follow the ideal response. The filter remains very close to the ideal one if the integrator phase at its unity-gain frequency ω_t is equal to its ideal value $-\pi/2$; the amount by which the phase at ω_t deviates from this quantity will be called $\Delta\varphi(\omega_t)$.

$$\varphi(\omega_t) = -\frac{\pi}{2} + \tan^{-1}\left(\frac{\omega_1}{\omega_t}\right) - \tan^{-1}\left(\frac{\omega_t}{\omega_2}\right) \Rightarrow \Delta\varphi(\omega_t) \approx \tan^{-1}\left(\frac{g_{out}}{g_m}\right) - \tan^{-1}\left(\frac{\omega_t}{\omega_2}\right) \tag{3}$$

Low dc-gain causes a leading phase error, and parasitic high-frequency poles and zeros in the integrator create lagging ($\omega_2>0$, RHP-zero) or leading ($\omega_2<0$, LHP-zero) phase errors. The acceptable worst case value of $\Delta\varphi(\omega_t)$ depends on the specifications for the high-frequency response of the overall filter and the poles and quality factor of the transconductor transfer function. The integrator phase error can be modelled with a frequency-dependent integrator quality factor Q_{int} (Nauta, 1993), concluding that a high and accurate filter quality factor puts strong constraints on the integrators phase error, i.e. on Q_{int}.

$$\frac{1}{Q_{\text{int}}(\omega)} \approx \Delta\varphi(\omega) = \frac{\omega_1}{\omega} - \frac{\omega}{\omega_2} \tag{4}$$

The filter performance is dominated by the performance of the transconductors, since the filter specifications (dynamic range, dissipation and chip area) depend not only on filter properties (Q, cut-off frequency, impedance level) but also on transconductor properties (A_{DC}, ω_t, ω_1, ω_2, noise behaviour, linearity, area and power consumption). It is therefore useful to put effort into the study of a high-performance transconductor that would improve all its specifications, in order to obtain a proper design for these VHF filter building blocks.

3. Fully-balanced pseudo-differential transconductor cell

In this section, the development of a fully-balanced current-mode integrator based on a classical structure is described, which is characterized by low-power, high rejection of supply noise and VHF potential application. Fig. 3 shows the conceptual scheme of the Zele-Smith pseudo-differential integrator (Smith et al., 1996; Zele et al., 1996), a complete fully-balanced transconductance cell arranged for using a current-mode integrator.

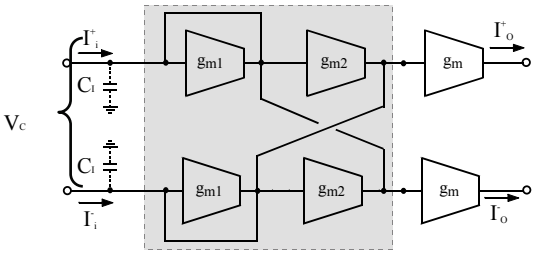


Fig. 3. Conceptual scheme of the complete fully-balanced current-mode transconductor.

To understand the basic operation we analyse the simple first-order model of the proposed transconductor, considering each unit cell as a simple transistor, i.e., single common-source stages as shown in Fig. 4. Under these conditions, the small-signal analysis gives the expression for the differential gain of the integrator (Eq. 5), where gmi is the i-cell transconductance and g_o' is the sum of output conductances g_{dsi} at the input node.

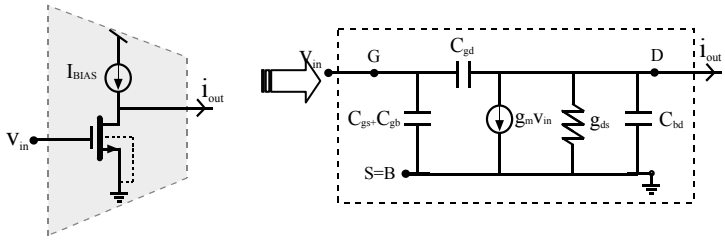


Fig. 4. Small-signal model for the common-source transconductor stage.

By analysing this expression and considering a first-order approximation, i.e., neglecting the g_{ds} effects of each transistor, an infinite dc-gain is achieved if perfect matching is obtained between g_{m1} and g_{m2}, so that $\delta g_m = g_{m1} - g_{m2} = 0$. Nevertheless, the effect of the output

conductances is not avoidable and the implementation of a negative resistance ($\delta g_m<0$), inherent to this topology, provides the possibility of achieving dc-gain enhancement. Note that by making $\delta g_m+g_o' \to 0$, then $|A_{DC}| \to \infty$. In practice, mismatching between transistors limits the differential gain by up to 55 dB at most. Another equivalent way for analysing this improvement is to consider the differential-mode input resistance of the transconductor cell.

$$A_{DC} = \left| \frac{I_O^+ - I_O^-}{I_i^+ - I_i^-} \right| \approx \frac{g_m}{g_{m1} - g_{m2} + g_o'} \cong \frac{g_m}{\delta g_m + g_o'}; \quad R_D(in) \approx \frac{2}{g_{m1} - g_{m2} + g_o'} = \frac{2A_{DC}}{g_m} \tag{5}$$

As a result, this scheme shows the basic pseudo-differential structure obtained by considering two dual transconductor cells (g_m), leading to current integration through input capacitance C_I. Thanks to the additional negative resistance shown in grey in the same figure, dc-gain is increased by providing positive feedback compensation for the signal current and boosting the input resistance of the transconductor.

The approximate common-mode gain, which must be less than unity to guarantee stability in closed-loop configurations, is constrained by device ratios to a stable value over all frequencies (Eq. 6). Common-mode stability is assured by designing $(g_{m1}+g_{m2})/g_m>1$. Common-mode behaviour analysis can be also carried out by calculating common-mode input resistance.

$$|A_{CM}| = \left| \frac{I_O^+ + I_O^-}{I_i^+ + I_i^-} \right| \approx \frac{g_m}{g_{m1} + g_{m2} + g_o'}; \quad R_{CM}(in) \approx \frac{1}{2\left(g_{m1} + g_{m2} + g_o'\right)} = \frac{|A_{CM}|}{2g_m} \tag{6}$$

The common-mode feedback resulting from the interconnection of the negative resistance provides both a naturally high differential gain and low common-mode gain for the integrator, improving these limits attached to a real integrator structure. Consequently, the basic operation of the transconductor will be best understood by explaining, first, that the common-mode control and dc-enhancement circuitry is connected at the input of the circuit and then, that the linear V-I conversion mechanism occurs in the output stage.

The gain of the basic current integrator is independent of the supply voltage to the first-order approximation. When fully-differential current topologies are used, the small remaining supply noise feedthrough is common to both sides of the signal and thus has no direct effect, except through random device mismatch. Therefore, the integrator has good immunity to supply noise. Device mismatch can be minimized with careful layout and specific design techniques to around 0.1-1 %, in many applications (Croon et al., 2002; Otin et al., 2004; Otin et al., 2005).

The use of an integrator based on transconductance cells implemented by using single transistors (no internal nodes), results in a proper frequency response because the only nodes are at the inputs and at the outputs. To a first-order approximation, no parasitic poles or zeros exist in the differential ac-response of the basic integrator circuit. Both differential and common-mode gains can be independently set by the different values of g_{m1} and g_{m2}. The ideal integrator function is a result of setting $\delta g_m+g_o'=0$ and the phase error at the unity-gain frequency, $\omega_t=g_m/C_I$, can be calculated by:

$$\Delta\varphi(\omega_t) = \tan^{-1}\left(\frac{\omega_1}{\omega_t}\right) \approx \tan^{-1}\left(\frac{\delta g_m + g_o'}{g_m}\right) = \frac{\pi}{2} - \tan^{-1}\left(\frac{g_m}{\delta g_m + g_o'}\right) \tag{7}$$

To summarize, infinite differential input impedance can be obtained if $\delta g_m+g_o' \rightarrow 0$ while maximizing the differential dc-gain and minimizing the phase error at ω_t, and common-mode input impedance can be reduced by maximizing the sum of the transconductances ($g_{m1}+g_{m2}$). Consequently, the common-mode rejection ratio (CMRR) is improved. Nevertheless, an important concept should be borne in mind: as the dc-gain depends on the difference ($g_o'-|\delta g_m|$), the structure can lead to instability if this quantity becomes negative (total negative input conductance) due to overcompensation.

By analysing the small signal model of each common-source stage forming the complete transconductor topology (Fig. 4), the need to solve a frequency problem arises: the feedforward ac-current path from the gate (input) to the drain (output), through the overlap parasitic capacitance C_{gd}. When considering the stages forming the negative resistance, the repercussion of this effect is not important because the contribution to the total behaviour of the cell decreases as these capacitances are short-circuited with their respective g_{mi}. However, the feedforward current through C_{gd} in the fully-balanced output-stage g_m of the transconductor structure generates a transmission zero (g_m/C_{gd}) in the right complex half-plane. This parasitic RHP-zero modifies the integrator frequency response and creates a phase-lag at the unity-gain frequency. Furthermore, the Miller effect, also associated with this parasitic capacitor, introduces larger equivalent input capacitance ($C_{in}=C_{gs}+C_{gb} \Rightarrow C_{in}=C_{gs}+C_{gb}+(1+A)C_{gd}$) and an additional component to the equivalent output capacitance ($C_{out}=C_{bd} \Rightarrow C_{out}=C_{bd}+(1+A^{-1})C_{gd}$), where $A \approx g_m/g_{ds}$. Therefore, the neutralization of this effect will involve bandwidth enhancement.

Many methods have been proposed to minimize the Miller effect: the cascode technique (Gray et al., 2001), the inductor shunt peaking technique (Mohan et al., 2000), the capacitive compensation technique (Wakimoto et al., 1990; Vadipour, 1993), the distributed amplification technique (Ahn et al., 2002) and the active inductor technique (Säckinger et al., 2000). They all have the advantages of low-voltage compatibility and low area; however, the solutions considered in this work will be the use of cascode structures together with the capacitive compensation technique.

Differential systems allow the C_c-cancellation technique, using positive feedback to generate negative capacitances, which can cancel the positive ones to yield bandwidth increases. These C_c capacitors are the overlap C_{gd} parasitic capacitances of dummy compensation transistors used in a cross-coupled way to neutralize the feedback action of these Miller capacitors. The connection is between the output and the opposite sign input, available in a balanced configuration. Under these conditions, the RHP-zero is moved to infinity, i.e., the cause of phase lag is removed, thus expanding the bandwidth of the transconductor. At the same time, compensation capacitor C_c will cancel the Miller effect and a lower input node effective capacitance is obtained due to the reduction of the feedforward effect. This technique depends on feeding back a current that is precisely the same as the one flowing through the Miller capacitance C_{gd} and, in consequence, the neutralization capacitor must match precisely. However, it is remarkable that C_{gd} is voltage-dependent and compensation can only work with small signals. In the case of mismatch between C_{gd} and C_c, parasitic zero is not at infinity and can cause a small phase lag or lead.

However, this is not the full story of the high frequency behaviour of the transconductor cell and there are more frequency limits. Mismatch in common-mode feedback circuits can result in unexpected parasitic poles and zeros. In addition, high frequency models of the MOS transistor show that g_m is not independent of frequency, but has a finite delay $g_m(s)$

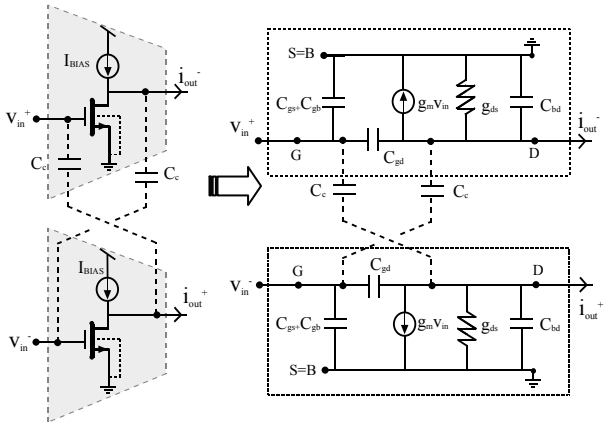


Fig. 5. Cancellation of transmission zero g_m/C_{gd} and neutralization of the Miller effect: C_c-cancellation technique.

and begins to roll off at very high frequencies. Although the frequency where this roll-off begins can be in the GHz range, the phase shift from this effect can become significant at much lower frequencies. Since most active filters are very sensitive to small phase changes in the integrator response, it is thus important to take this effect into account.

The first way to minimize these effects is to eliminate the internal nodes or, if this is not possible, to design them as low-impedance nodes. This procedure can be carried out by considering cascode topologies. Moreover, their use further prevents bandwidth reduction generated by transmission zero because one side of C_c is connected to the internal low-impedance node, i.e., to the low-gain point of the cascode transistor source.

Therefore, an enhancement of the integrator dc-gain has been obtained with this topology by means of the differential negative resistance, increasing the differential input resistance of the transconductor and keeping the common-mode gain lower than unity. With regard to frequency limit-related problems, transmission zero has been reduced by using C_c-capacitor compensation, taking advantage of the pseudo-differential topology. This solution can also be improved by considering cascode topologies, giving higher dc-gains in a natural way, which will also reduce the frequency drawbacks associated to the internal nodes of other topologies by avoiding internal high-impedance nodes in the signal path.

As a result, a low-voltage transconductor with high linearity, very high operation frequency and high power efficiency has been designed where cascode structures should be considered to obtain an improvement in the high-frequency behaviour of the basic topology. The main advantage of using cascode stages instead of single common-source stages is the higher dc-gain while maintaining a good frequency response. Hence, a higher quality factor of the integrator is expected due to the higher differential dc-gain (Abidi, 1988). Basic cascode circuits require high supply voltages to operate due to the large overhead bias from threshold voltages. However, variations of the cascode technique exist which can be used with lower voltage supplies. Two options are considered in this work, the so-called **high-swing cascode (HS)** stage and the **folded cascode (FC)** stage (Baker et al., 1998; Sansen et al. 1999; Sedra et al., 2004). The unit cells replacing the common-source stages previously used are shown in Fig. 6. The complete fully-balanced current-mode transconductance cells implemented by using these cascode stages are described in the following sections.

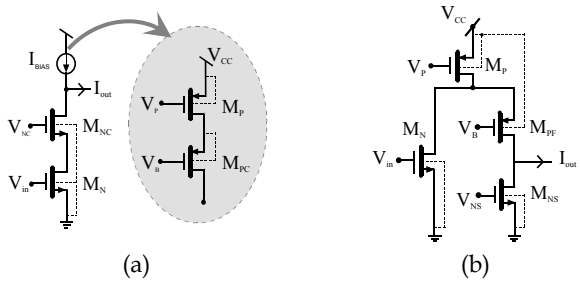


Fig. 6. Unit transconductance cell: (a) high-swing (HS) and (b) folded cascode (FC) topology.

3.1 High-swing cascode section: HS topology

Fig. 7(a) shows the transconductor arranged for using the current-mode integrator described in Fig. 3, where the unit cells have been implemented by using high-swing cascode stages (Baker et al., 1998; Sansen et al. 1999; Sedra et al., 2004). As illustrated in the corresponding HS unit cell (Fig. 6(a)), current sources are also implemented by using high-swing cascode elements. The substrate terminals of NMOS transistors are connected to the reference voltage as usual, and those of the PMOS transistors are connected to the corresponding source node of each transistor.

The use of high-swing cascode elements offers as high accuracy as using basic cascode stages to implement each unit cell of the transconductor but, because of the slightly different connection between transistors, needs lower supply voltage and has fewer internal parasitic poles, generating nodes between the input and the output, giving a better frequency response of the integrator. The main disadvantage of the improved cascode topology is that due to biasing constraints, the gate-source voltages must be kept small, resulting in larger devices for a bias current level.

3.2 Folded cascode section: FC topology

In order to obtain an improvement in biasing flexibility and further reduction of the supply voltage in the design of the transconductor cell, we can also take advantage of folded-cascode sections (Sansen et al. 1999; Sedra et al., 2004). The schematic used to describe the complete integrator based on the proposed current-mode pseudo-differential transconductor is shown in Fig. 7(b), where the unit cells have been implemented by using FC stages illustrated in Fig. 6(b). In this case, current sources are implemented by using single elements, both bias sources I_{BIAS} and cascode sources M_{NSi}. The substrate terminals of NMOS transistors are connected to the reference voltage as usual, and those of PMOS transistors, both those used to implement current sources I_{BIAS} and those implementing folded transistors M_{PFi}, are connected to the V_{CC} node.

The use of folded cascode elements exhibits a substantial improvement in biasing flexibility, because of the increased drain-voltage of the transistors, at the cost of additional current sources and bias voltages. Another significant benefit of using these stages is that by avoiding the biasing constraints associated to the high-swing cascode structure, we obviate the need to keep gate-source voltages low, which results in smaller and simpler devices for a given bias current level, lower voltage supply and larger unity-gain frequencies.

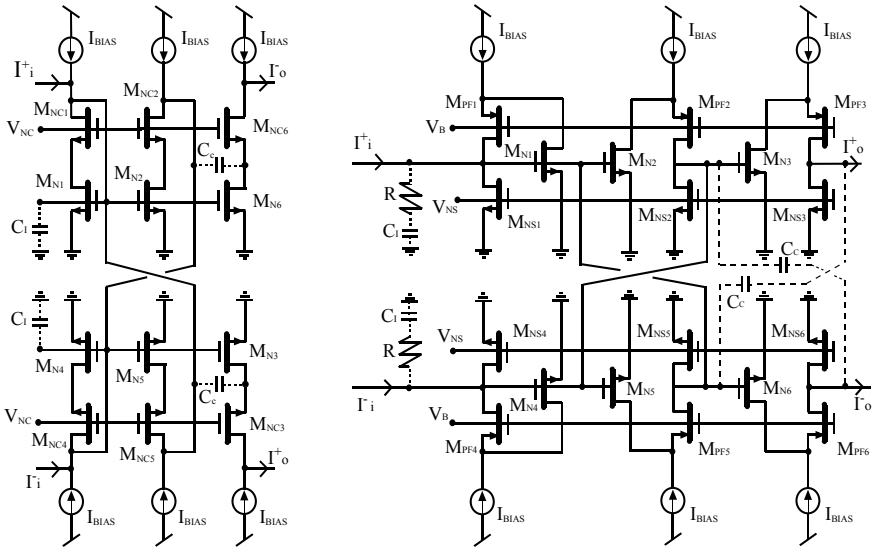


Fig. 7. Fully-balanced pseudo-differential current-mode cell, based on (a) high-swing cascode unit stages: **HS transconductor**; (b) folded-cascode unit stages: **FC transconductor**.

3.3 General considerations: basic principle

A similar notation and index-linking have been adopted in both transconductor implementations in order to simplify the description of the basic principle and to unify the topology analysis. Assuming ideal behaviour for the integrator, the balanced input current flows entirely into integration capacitance C_I. Diode-connected stages $M_{1,4}$ adequately bias cascode output $M_{3,6}$, whilst transistors $M_{2,5}$ provide positive feedback compensation for the signal current flowing into $M_{1,4}$ and boost the input resistance of the integrator.

Regarding the gain enhancement by means of the negative resistance formed by transistors $M_{2,5}$, this technique is absolutely necessary for Zele-Smith topologies and other voltage-mode transconductors (Nauta, 1993), in order to obtain reasonably high dc-gain values. Theoretically, the dc-gain could be infinity by adjusting the equivalent negative resistance, but in practice mismatching limits the dc-gain by about 40 dB in single transistor stages. However, the use of cascode topologies leads to a natural enhancement of this parameter and differential dc-gain values of up to 55 dB can be reached with identical transistors under identical bias conditions by means of a lower mismatching sensitive design. Nevertheless, there is a key difference between the HS and the FC cascode structure:

- The high output resistance is directly guaranteed thanks to the true cascode output stage exhibited by the HS transconductor. Therefore, positive feedback compensation is not necessary to boost differential resistance or enhance the dc-gain.
- On the other hand, the output-node for the FC transconductor is not a very high impedance node, and the negative resistance proves necessary to obtain real input resistance enhancement. In this approach, positive feedback compensation for the signal current flowing into $M_{3,6}$ is essential, boosting the input resistance of the integrator and increasing dc-gain.

The reason for this difference is that the FC unit cell considered and shown in Fig. 6(b) is a pseudo-cascode topology. To obtain similar output impedance to that of the HS approach, the M_{NS} current source would have to be implemented by using a cascode current source. Nevertheless, even if the HS implementation undergoes an immediate dc-gain/input resistance improvement, both topologies require positive feedback compensation (negative resistance) to reduce common-mode gain (common-mode input resistance) and stabilize common-mode voltages. On the other hand, the use of pseudo-differential structures requires careful and efficient control over the common-mode behaviour of the circuit. It is worth noting that this structure not only stabilises the common-mode voltage, but also rejects common-mode signals by means of partial positive feedback. This idea has already been used for high-frequency transconductors in (Nauta, 1993) and for a class of current-mode filters (Smith et al., 1996; Zele et al., 1996).
Thus, considering this topology implemented by using cascode stages, dc-gains of about 55 dB and CMRR of 60 dB can be obtained with inherent stability of common-mode voltages. Note that the propagation of common-mode (CM) signals in balanced circuits can cause instability and distortion. Further, current consumption, linearity and transconductance value are strongly dependent on the CM input signals. Additional techniques can be used in the proposed topology if a greater CMRR is needed, such as feedforward cancellation of the input CM signal. Balanced transconductors with high-input common-mode rejection that are capable of operating with low-voltage supplies are obtained by using an additional transconductor that is only sensitive to CM signals (Baschirotto et al., 1994; Wyszynski et al., 1994). Considering this technique, CMRR values up to 70 dB could be obtained.

4. High frequency response

In this section, the bandwidth of the transconductor will be analysed. Note that if single transistor stages and unrealistic simplified models are used in the proposed topology (Fig.3), the bandwidth could be infinite owing to the absence of internal nodes influencing the transfer function of the integrator. A more complete model of the MOS transistor does predict a finite bandwidth due to the second-order frequency effects such as the transmission zero associated to overlap parasitic capacitance C_{gd}, frequency dependence of the transconductance $g_m(s)$ and mismatch in common-mode feedback circuits. A closer explanation of MOS behaviour at high-frequencies (splitting it into an **intrinsic** and an **extrinsic** part) is required before starting the study of the complete integrator. Taking into account a non-quasistatic model (Tsividis, 1996), the high-frequency behaviour of the current mode integrator will be calculated.
When analysing transconductor bandwidth, several general factors must be considered:

- The output of the complete transconductor may be assumed to be short-circuited for ac-signals when calculating the frequency response of the integrator.
- In all the equations: g_m is the transconductance, g_{ds} the output conductance, g_{mb} the bulk-transconductance and C_{gd}, C_{gs}, C_{ds}, C_{bs} and C_{bd} the parasitic capacitances.
- All the unit cells are designed to seek perfect matching between them. Therefore, all similar transistors have the same properties except for transconductance g_m of the N-transistor processing the signal (M_N transistor in both unit cells shown in Fig. 6). In this way, considering the notation and index-linking previously used in Fig. 3: $g_m(N_1)=A_N g_m(N)$; $g_m(N_2)=A_P g_m(N)$; $g_m(N_3)=g_m(N)$. Consequently, $\delta g_m=(A_N-A_P)g_m$

represents the difference between M_1 and M_2, or, M_4 and M_5 due to the difference in dimensions and bias currents of N-transistors, which gives rise to the negative resistance that enhances the dc-gain of the system.

- Total integration capacitance C_I comprises not only the external capacitance, but also the contribution of parasitic capacitors (C_I=C_{ext}+C_p). Intrinsic capacitance C_{gs} is the main contribution of these parasitic capacitances C_p and consideration of it as a great percentage of total integration capacitance acquires great significance.
- External capacitor C_{ext} can be implemented by using double-poly, metal-metal or MOS capacitors, depending on the technological process.
- Current source is modelled with a Norton equivalent circuit, where G_s and C_s are the admittance and capacitance components. The external capacitance C_{ext} connected to the transconductor input is in parallel with C_s. For purposes of simplicity, from now on, C_s will include the equivalent capacitance of the current source and the external capacitance (C_s≡C_s+C_{ext}). Therefore, total integration capacitance can be expressed as: C_I=C_s+C_p, including parasitic effects, the external capacitance and the equivalent-model of the non-ideal current source.

Firstly, a model for the V-I conversion of the unit cell is derived, in both implementations to show the calculation process of the bandwidth of the complete transconductance cell.

4.1 High-frequency model of the HS unit cell

The following circuit represents the high frequency model for the HS unit cell previously shown in Fig. 6(a), where X(N) denote the parameters associated to the M_N-transistor, X(NC) those associated to the cascode transistor, X(P) those associated to current sources I_{BIAS} and X(PC) those associated to the cascode current sources as shown in Fig. 6(a). Table 1 summarizes the parameters associated to the impedances shown in the small-signal equivalent circuit. The rest of the elements: g_m(N), g_{ds}(N), g_{ds}(NC), g_{ds}(PC), g_m(PC), C_{gd}(N) and C_{ds}(NC) directly represent the parameters of the respective transistor.

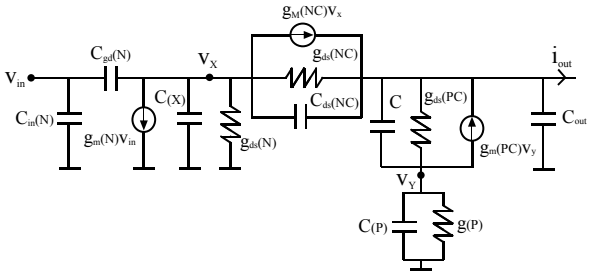


Fig. 8. Equivalent high-frequency circuit for the HS unit cell.

$g_M(NC) = g_m(NC) + g_{mb}(NC)$	$g(P) = g_{ds}(P)$
$C_{in}(N) = C_{gs}(N) + C_{gb}(N)$	$C(x) = C_{ds}(N) + C_{bd}(N) + C_{gs}(NC) + C_{bs}(NC)$
$C = C_{ds}(PC) + C_{bd}(PC)$	$C_{out} = C_{gb}(NC) + C_{bd}(NC) + C_{gd}(PC)$
$C(P) = C_{gd}(P) + C_{ds}(P) + C_{bd}(P) + C_{gb}(PC) + C_{gs}(PC)$	

Table 1. Small-signal parameters for the HS unit cell.

4.2 High-frequency model of the FC unit cell

The following circuit represents the high frequency model for the FC unit cell previously shown in Fig. 6(b), where X(N) are the parameters associated to the M_N-transistor, X(PF) those associated to the folded transistor, X(P) those associated to the current sources I_{BIAS} and X(NS) those associated to the current source of the folded transistor, which is implemented with a single NMOS transistor as previously illustrated.

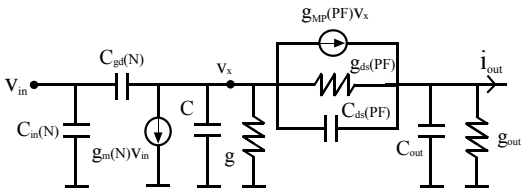


Fig. 9. Equivalent high-frequency circuit for the FC unit cell.

Table 2 summarizes the parameters associated to the impedances shown in the small-signal equivalent circuit. The rest of the elements: $g_m(N)$, $g_{ds}(PF)$, $C_{gd}(N)$ and $C_{ds}(PF)$ directly represent the parameters of the respective transistor.

$g = g_{ds}(N) + 2g_{ds}(P)$	$C_{in}(N) = C_{gs}(N) + C_{gb}(N)$
$g_{out} = g_{ds}(NS)$	$C = C_{ds}(N) + C_{bd}(N) + 2C_{gd}(P) + 2C_{ds}(P) + 2C_{bd}(P) + C_{gs}(PF) + C_{bs}(PF)$
$g_{MP}(PF) = g_m(PF) + g_{mb}(PF)$	$C_{out} = C_{gd}(PF) + C_{bd}(PF) + C_{gd}(NS) + C_{ds}(NS) + C_{bd}(NS)$

Table 2. Small-signal parameters for the FC unit cell.

Great similarity is obtained in the description of both unit cells. Even the FC capacitive parameter C will be equivalent to C+C(x) in the HS description. This parallelism will also appear in the complete transconductor analysis.

4.3 High-frequency model of the complete transconductance cell

Under these conditions, the differential gain of the proposed transconductor cell (in both implementations) can be calculated by:

$$H(s) = k\frac{(s-s_0)(s+s_1)}{s^2 + x_1 s + x_2} \approx K\frac{(s-s_0)}{(s+\delta_1)(s+\delta_2)} \tag{8}$$

where:

$$K = \frac{-A_{DC}\,\delta_1\,\delta_2}{s_0}; \quad x_1 = \frac{\beta}{\gamma}; x_2 = \frac{\alpha}{\gamma}; \quad \delta_1 = \frac{\alpha}{\beta} = \frac{x_2}{x_1}; \quad \delta_2 = \frac{\beta}{\gamma} - \delta_1 \approx \frac{\beta}{\gamma} = x_1 \tag{9}$$

Denominator factorization of Eq.(8) leads to obtain two parasitic poles, $-\delta_1$ and $-\delta_2$, but only if the approximation $(\alpha\cdot\gamma/\beta^2)<<1$ is verified. Furthermore, parasitic zero $-s_1$ must be negligible in the frequency range of interest. Both considerations will be demonstrated, either in the HS or in the FC approach ($s_1>>s$ and $s_1>>s_0$: s_1(HS)=1600 s_0=1100 GHz, s_1(FC)=30 s_0=1900 GHz).

Due to the use of a pseudo-differential structure, a careful study of the common-mode behaviour is mandatory. Thanks to the topology proposed, the common-mode voltage is

stabilized by means of partial positive feedback as previously explained. Under these assumptions:

$$A_{CM}(s) = k_{CM}\frac{(s-s_0)(s+s_1)}{s^2+y_1 s+y_2} \approx K_{CM}\frac{(s-s_0)}{s^2+y_1 s+y_2} \tag{10}$$

$$K_{CM} = \frac{-A_{CM}\, y_2}{s_0}; \quad y_1 = \frac{\beta_{CM}}{\gamma_{CM}}; y_2 = \frac{\alpha_{CM}}{\gamma_{CM}} \tag{11}$$

Eq.(10) once more shows the need to neglect parasitic zero $-s_1$, leading to the same consideration as in the differential gain equation. In this analysis, denominator factorization is more difficult to accomplish. However, the approximate equations are easily derived and, making use of the figures obtained in each particular design, the possibility of using the approximate common-mode transfer function will be analysed. Therefore, if $(\alpha_{CM}\cdot\gamma_{CM}/\beta_{CM}^2)<<1$ is verified, the common-mode gain can be expressed as:

$$A_{CM}(s) = K_{CM}\frac{(s-s_0)}{(s+\xi_1)(s+\xi_2)} \tag{12}$$

$$\xi_1 = \frac{\alpha_{CM}}{\beta_{CM}} = \frac{y_2}{y_1}; \quad \xi_2 = \frac{\beta_{CM}}{\gamma_{CM}} - \xi_1 \approx \frac{\beta_{CM}}{\gamma_{CM}} = y_1 \tag{13}$$

Both transfer functions are characterized by two parasitic poles and one RHP-zero; the differential-mode by $-\delta_1$, $-\delta_2$, and s_0; and the common-mode by $-\xi_1$, $-\xi_2$, and s_0 (zero s_0 is the same in both transfer functions)[1]. Consequently, in order to obtain a transconductor design that is compatible with all the requirements of the active G_m-C filter implementation, a proper analysis and characterization of these parasitic elements becomes a top-priority challenge. From this study, their origin and frequency location may lead to some design considerations to improve the integrator frequency response.

Differential dc-gain, common-mode dc-gain, s_0 and s_1 are summarized in table 3 for both implementations. The parasitic poles can be calculated by using α, β, γ, α_{CM}, β_{CM}, γ_{CM}, as shown in Eqs.(9) and (13). As the resulting relations are very complicated, it is necessary to look for the dominant terms and obtain approximate expressions to draw conclusions. They can be simplified to analyse and understand the behaviour of the transconductance cell and its frequency limits that are associated to second order effects, which differentiate between the frequency behaviour of the proposed topology and the expected ideal response.

4.4 HS transconductance cell frequency response

Considering the previous study of the HS unit cell, a detailed analysis of the frequency response of the complete HS integrator is carried out. The dominant terms of these expressions are subsequently obtained in this section. In order to simplify the notation, the small-signal parameters are redefined in table 4.

[1] According to stable systems, negative poles $-\delta_1$, $-\delta_2$, $-\xi_1$ and $-\xi_2$ have been obtained in the transfer functions for both implementations. For purposes of simplicity, when referring to these poles, their associated frequency (δ_1, δ_2, ξ_1, ξ_2) will be the considered magnitude.

	HS transconductor	FC transconductor
S_0	$s_0 = \frac{g_m(N)}{C_{gd}(N)}$	$s_0 = \frac{g_m(N)}{C_{gd}(N)}$
S_1	$s_1 = \frac{g_M(NC) + g_{ds}(NC)}{C_{ds}(NC)}$	$s_1 = \frac{g_{MP}(PF) + g_{ds}(PF)}{C_{ds}(PF)}$
A_{DC}	$A_{DC} = \frac{g_m(N)\left(g_M(NC) + g_{ds}(NC)\right)}{\alpha}$	$A_{DC} = \frac{g_m(N)\left(g_{MP}(PF) + g_{ds}(PF)\right)}{\alpha}$
A_{CM}	$A_{CM} = \frac{-g_m(N)\left(g_M(NC) + g_{ds}(NC)\right)}{\alpha_{CM}}$	$A_{CM} = \frac{-g_m(N)\left(g_{MP}(PF) + g_{ds}(PF)\right)}{\alpha_{CM}}$

Table 3. Summary of the high-frequency parameters.

$G = g_{ds}(N) + g_M(NC) + g_{ds}(NC)$
$C_{IN} = C_s + 2C_{in}(N) + C_{out} = C_s + 2C_{gs}(N) + 2C_{gb}(N) + C_{gb}(NC) + C_{bd}(NC) + C_{gd}(PC)$
$C_\beta = C_{out} + C_{in}(N) = C_{gs}(N) + C_{gb}(N) + C_{gb}(NC) + C_{bd}(NC) + C_{gd}(PC)$

Table 4. Impedance parameters for the HS integrator.

By analysing in detail the small-signal equivalent model for the complete HS integrator, the value of total integration capacitance C_I can be calculated by Eq.(14). This definition will lead to a simplification of the parasitic pole expressions.

$$C_I = C_{IN} + C_\beta = C_s + 3C_{in}(N) + 2C_{out} \tag{14}$$

Firstly, the differential and common-mode gain can be expressed as follows:

$$A_{DC} \approx \left[\left(A_N - A_P\right) + \frac{2g_{ds}(NC)g_{ds}(N)}{g_m(N)\left(g_M(NC) + g_{ds}(NC)\right)} \right]^{-1} \tag{15}$$

$$A_{CM} \approx -\left[\left(A_N + A_P\right) - \frac{2g_{ds}(NC)g_{ds}(N)}{g_m(N)\left(g_M(NC) + g_{ds}(NC)\right)} \right]^{-1} \approx \frac{-1}{A_N + A_P} \tag{16}$$

In these expressions, the differential negative resistance obtained by the partial positive feedback compensation is shown by means of the difference $\delta g_m=(A_N-A_P)g_m(N)$. The existence of this negative resistance allows the differential dc-gain to be enhanced. Parasitic poles δ_1 and δ_2 can be calculated by means of ratios between α, β and γ. Final expressions are summarized in table 6. The origin of second order effects can be better understood by focusing on their dependence.

$$\alpha \approx \left(\left(A_N - A_P\right)g_m(N)\right)\left(g_M(NC) + g_{ds}(NC)\right) + 2g_{ds}(NC)g_{ds}(N) \approx 2g_{ds}(NC)g_{ds}(N) \tag{17}$$

$$\beta \approx G\left(C_s + 3C_{in}(N) + 2C_{out}\right) = G\,C_I \tag{18}$$

where considering the dominant term in the transconductance G, the expression can be written as:

$$\beta \approx \left(g_{ds}(N) + g_M(NC) + g_{ds}(NC)\right)C_I \approx g_M(NC)\,C_I \tag{19}$$

Therefore, the parasitic pole δ_1 can be expressed as:

$$\delta_1 = \frac{\alpha}{\beta} \approx \frac{2g_{ds}(NC)g_{ds}(N)}{g_M(NC)\,C_I} \tag{20}$$

Following the same process for the other pole δ_2, we obtain:

$$\gamma \approx C_I\left(C_{gd}(N) + C_{ds}(NC) + C(x)\right) \approx C_I\,C(x) \approx C_I\,C_{gs}(NC) \tag{21}$$

$$\delta_2 = \frac{\beta}{\gamma} \approx \frac{G}{C(X)} = \frac{g_{ds}(N) + g_M(NC) + g_{ds}(NC)}{C_{ds}(N) + C_{bd}(N) + C_{gs}(NC) + C_{bs}(NC)} \approx \frac{g_M(NC)}{C_{gs}(NC)} \tag{22}$$

Similar results can be obtained for the common-mode frequency response:

$$\alpha_{CM} \approx \left(\left(A_N + A_P\right)g_m(N)\right)\left(g_M(NC) + g_{ds}(NC)\right) \approx \left(A_N + A_P\right)g_m(N)g_M(NC) \tag{23}$$

$$\beta_{CM} \approx \beta \approx g_M(NC)\,C_I; \quad \gamma_{CM} \approx \gamma \approx C_I\;C_{gs}(NC) \tag{24}$$

$$\xi_1 = \frac{\alpha_{CM}}{\beta_{CM}} \approx \frac{(A_N + A_P)g_m(N)g_M(NC)}{G\,C_I} \approx \frac{(A_N + A_P)g_m(N)}{C_I}; \quad \xi_2 = \frac{\beta_{CM}}{\gamma_{CM}} \approx \delta_2 \approx \frac{G}{C(X)} \approx \frac{g_M(NC)}{C_{gs}(NC)} \tag{25}$$

4.5 FC transconductance cell frequency response

Considering the previous study of the FC unit cell, a detailed analysis of the frequency response of the complete FC integrator is carried out. The dominant terms of these expressions are obtained in this section. In order to simplify the notation, two small-signal parameters are redefined in table 5.

$G_I = G_s + 2g_{out}$
$C_I = C_s + 3C_{in}(N) + 2C_{out} = C_s + 3C_{gs}(N) + 3C_{gb}(N) + 2C_{gd}(PF)$ $+ 2C_{bd}(PF) + 2C_{gd}(NS) + 2C_{ds}(NS) + 2C_{bd}(NS)$

Table 5. Impedance parameters for the FC integrator.

In accordance with the analysis of the small-signal equivalent model for the complete FC integrator, parameter C_I, defined in table 5, directly represents the total integration capacitance, the expression of which is the same as in the HS integrator. Therefore, the total integrator capacitance of both integrator implementations can be calculated by Eq.(26).

$$C_I = C_s + 3C_{in}(N) + 2C_{out} \tag{26}$$

For the FC integrator, the differential and common-mode gain can be expressed as follows:

$$A_{DC} \approx \left[\left(A_N - A_P\right) + \frac{2g_{ds}(NS)\left(g_{MP}(PF) + 2g_{ds}(P)\right)}{g_m(N)\left(g_{MP}(PF) + g_{ds}(PF)\right)} \right]^{-1} \approx \left[\left(A_N - A_P\right) + \frac{2g_{ds}(NS)}{g_m(N)} \right]^{-1} \quad (27)$$

$$A_{CM} \approx -\left[\left(A_N + A_P\right) + \frac{2g_{ds}(NS)}{g_m(N)} \right]^{-1} \approx \frac{-1}{A_N + A_P} \quad (28)$$

In these expressions, the negative resistance obtained by the partial positive feedback compensation is shown again by means of the difference $\delta g_m=(A_N-A_P)g_m(N)$. Parasitic poles, δ_1 and δ_2, are obtained by means of ratios among α, β and γ, as in the HS implementation. The final expressions are summarized in table 6. Consequently, parasitic poles δ_1 and δ_2 can be expressed as:

$$\begin{aligned} \alpha &\approx \left(\left(A_N - A_P\right) g_m(N)\right)\left(g_{MP}(PF) + g_{ds}(PF)\right) + 2g_{ds}(NS)\left(g_{MP}(PF) + 2g_{ds}(P)\right) \approx \\ &\approx 2g_{ds}(NS)\left(g_{MP}(PF) + 2g_{ds}(P)\right) \end{aligned} \quad (29)$$

$$\beta \approx \left(g + g_{ds}(PF) + g_{MP}(PF)\right) C_I \approx \left(g_{MP}(PF) + 2g_{ds}(P)\right) C_I \quad (30)$$

$$\delta_1 = \frac{\alpha}{\beta} \approx \frac{2g_{ds}(NS)}{C_I} \quad (31)$$

$$\begin{aligned} \gamma &\approx C_I \left(C_{ds}(PF) + C_{gd}(N) + C\right) \approx C_I C \approx \\ &\approx C_I \left(2C_{gd}(P) + 2C_{ds}(P) + C_{gs}(PF) + C_{bs}(PF)\right) \approx 2\, C_I\, C_{gd}(P) \end{aligned} \quad (32)$$

$$\delta_2 = \frac{\beta}{\gamma} \approx \frac{g_{MP}(PF) + 2g_{ds}(P)}{2C_{gd}(P) + 2C_{ds}(P) + C_{gs}(PF) + C_{bs}(PF)} \approx \frac{g_{MP}(PF) + 2g_{ds}(P)}{2C_{gd}(P)} \quad (33)$$

Similar results can be obtained for the common-mode frequency response:

$$\begin{aligned} \alpha_{CM} &\approx \left(\left(A_N + A_P\right) g_m(N)\right)\left(g_{MP}(PF) + g_{ds}(PF)\right) + 2g_{ds}(NS)\left(g_{MP}(PF) + 2g_{ds}(P)\right) \approx \\ &\approx \left(A_N + A_P\right) g_m(N)\left(g_{MP}(PF) + g_{ds}(PF)\right) \end{aligned} \quad (34)$$

$$\beta_{CM} \approx \beta \approx \left(g_{MP}(PF) + 2g_{ds}(P)\right) C_I; \qquad \gamma_{CM} \approx \gamma \approx 2\, C_I\, C_{gd}(P) \quad (35)$$

$$\xi_1 = \frac{\alpha_{CM}}{\beta_{CM}} \approx \frac{(A_N + A_P) g_m(N)}{C_I}; \qquad \xi_2 = \frac{\beta_{CM}}{\gamma_{CM}} \approx \delta_2 \approx \frac{g_{MP}(PF) + 2g_{ds}(P)}{2C_{gd}(P)} \quad (36)$$

4.6 Comments and discussion

A full analysis has been developed in previous sections in order to draw some design strategies and implement a competitive and robust transconductor cell. Great similarity was found between the two topologies, as reflected in table 6.

The first conclusion regards total integration capacitance, C_I, which has the same definition in both implementations: $C_I=C_s+3C_{in}(N)+2C_{out}$ (Eq. 26), where C_s represents the equivalent