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Ultra wideband oscillators

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1. Ultra Wideband Oscillators

1.1 Introduction

Ultra wideband (UWB) wireless technology has promoted designing devices covering wide bandwidth over several gigahertz. Among them are UWB oscillators that should achieve very wide tuning range along with low phase noise performance.

An effective solution to this has been to use multiple narrowband VCOs, each covering a portion of the required range. This solution requires high cost and increased design complexity. Alternatively, varactors, switched capacitors, variable inductors, and tunable active inductors are proposed to extend the tuning range of VCOs. However, there are several challenges in realizing integrated VCOs with these techniques.

This chapter deals with the analysis and design of integrated oscillator circuits, with emphasis on Ultra Wideband (UWB) application. First, VCO fundamentals are introduced and the impacts of wideband operation on VCO performance are discussed. After that, the general guidelines in doing layout for active and passive devices will be presented. Focus will be placed on the optimum RF performance of components. Then, the design considerations along with various tuning methods for wideband oscillation will be introduced. In each case, the achieved tuning range realized through these methods is mentioned. Finally, the design and implementation of two Ultra wideband (UWB) VCOs are described, with the experimental results in a 0.18-µm CMOS technology.

1.2 Specification of Oscillator Properties

The most critical performance specification for an oscillator is its spectral purity, usually characterized by phase noise. In a receiver, the phase noise of the local oscillator (LO) degrades the received signal-to-noise ratio (SNR) of the desired signal at IF by a process often referred to as reciprocal mixing. This limits the ability to detect a weak signal in the presence of a strong signal in an adjacent channel. Phase noise also corrupts the information present in phase-modulated signals by effectively rotating the symbol constellation, degrading the bit error rate (BER) of communication systems. In a transmitter, LO phase noise is modulated onto the desired signal and results in energy being transmitted outside of the desired band.

Since many wireless transceivers are battery-powered, it is required to minimize the power consumption in oscillator. There is a trade-off between phase noise and power consumption until the voltage swing is maximized. Beyond this swing level, raising the current will increase the phase noise, and will waste power.

1.3 Single Transistor Oscillator

Colpitts and Hartley oscillators are two most popular single transistor topologies, as illustrated in Figure 1. The Colpitts oscillator has a capacitively tapped resonator, with a positive feedback provided by an active device.

In Hartley oscillator, the LC network has two inductors and one capacitance. The NMOS amplifier is connected in a common gate configuration. The capacitance C3 has one port connected to L1 and the other port connected to L2. There is no way to replace this capacitance with the load capacitance.

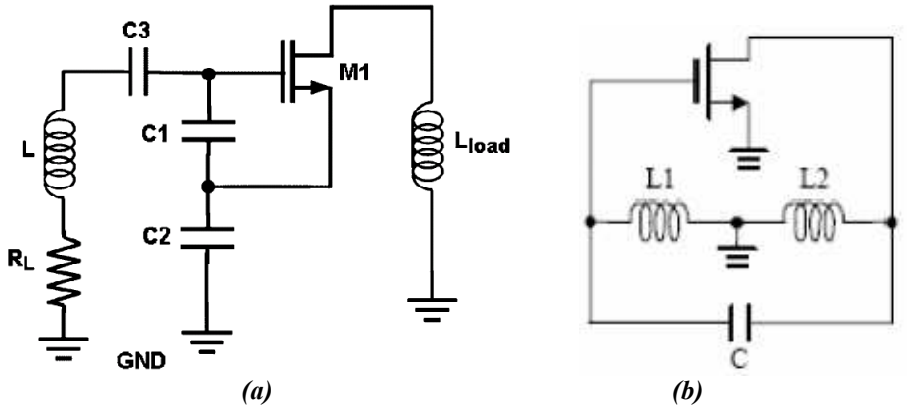


Fig. 1. AC equivalent circuit a) Colpitts VCO with a load inductor **b)** Hartley Oscillator

1.4 Differential Oscillators

The single-switch VCO (SS-VCO) and the double-switch VCO (DS-VCO) are two popular topologies used in the design of integrated oscillators. Figure 2 shows the simplified circuit schematic of both topologies. The transconductance in both circuits, which is set by the bias condition and the dimensions of the cross-coupled pair transistors, provides a negative resistance to compensate the losses in the resonator.

To control the negative resistance and hence set the oscillation amplitude, a tail current source is employed (transistor M3 in Fig. 2(a) and (b)). The presence of the tail current source, which reduces the oscillation headroom, affects the up-conversion of 1/f and thermal noise to phase noise as well [1].

In the SS-VCO two integrated inductors or a single center-tapped differential inductor may be employed, while a single center-tapped can be used in the DS-VCO. The parasitic capacitances associated with the transconductor cell are larger in the DS-VCO than in the SS-VCO. The parasitic capacitances reduce both the tuning range and the maximum oscillation frequency. The oscillation amplitude of the DS-VCO, for identical resonators and equal power consumption, is anticipated to be twice as large as in the SS-VCO [2]. Thus, DS-

VCO exhibits better phase noise performance compared to the SS-VCO. However, the former requires a larger supply voltage than the latter, due to the additional stacking of the PMOS pair.

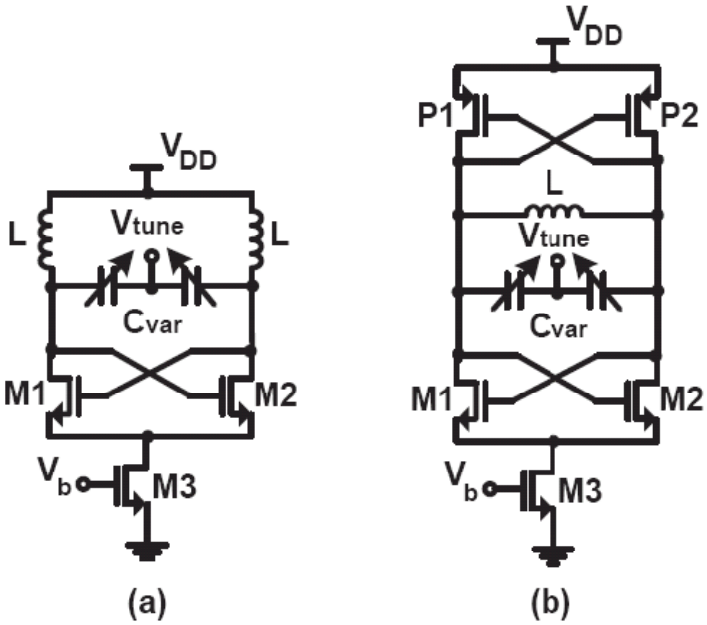


Fig. 2. Simplified circuits schematic of (a) the SS-VCO and (b) the DS-VCO.

1.5 Phase Noise

The most critical performance specification for an oscillator is its spectral purity. In any practical oscillator, the spectrum has power distributed around the desired oscillation frequency ω_0, known as *phase noise,* in addition to power located at harmonic frequencies, as shown in Figure 3.

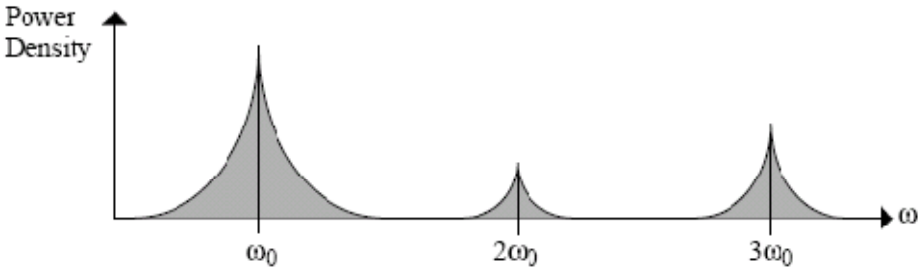


Fig. 3. Practical oscillator spectrum.

An oscillator can usually either be viewed as a single two-port feedback circuit, or as two one-port circuits connected together. Consider the linear feedback model depicted in Figure 4.

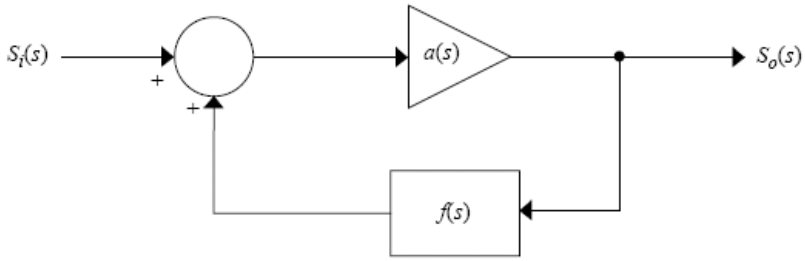


Fig. 4. Basic Oscillator feedback model

The overall transfer function from input to output is given by

$$\frac{S_o(s)}{S_i(s)} = \frac{a(s)}{1 - a(s)f(s)} \tag{1}$$

This system can have a non-zero output without any input as long as the quantity *a(s)f(s)*, i.e. the *loop gain*, is one and the phase shift around the loop is zero.
However, an initial loop gain magnitude greater than one is typically designed and then nonlinearities in the amplifier will reduce the magnitude to exactly one in steady-state operation.
Assuming *a(s)* has zero phase shift, we can implement *f(s)* as a resonator, realized with a parallel *LC* tank, having zero phase shift at the desired oscillation frequency.

Another way to view an oscillator is to break it up into two one-port networks, an active circuit and a resonator, as depicted in Figure 5. When the equivalent parallel resistance R_T of the resonator is exactly balanced by a negative resistance $-R_a$ of the active circuit, the negative resistance compensates the losses in the resonator and steady-state oscillation is achieved.

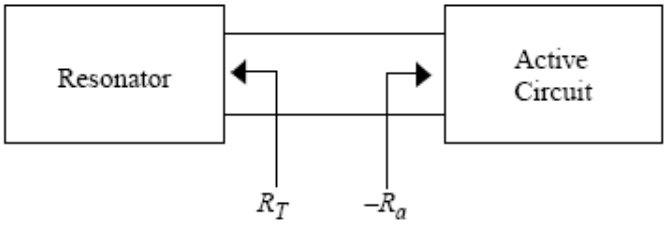


Fig. 5. Two One-port networks view of an oscillator.

1.5.1 One-Port View of Phase Noise

Figure 6 shows an equivalent one-port model of an *LC* oscillator, in which $i_n(\omega)$ denotes all noise sources in the circuit. Suppose the mean square noise current density is $\bar{i}_n^2/\Delta\omega$.

Assuming linear time-invariant behavior, total noise power density $P_n(\omega)/\Delta\omega$ can be calculated as [1]:

$$\frac{P_n(\omega)}{\Delta(\omega)} = \frac{\bar{\imath}_n^2}{\Delta(\omega)} \cdot |Z(\omega)| \tag{2}$$

where, $|Z(\omega)|$ is the tank's magnitude response.

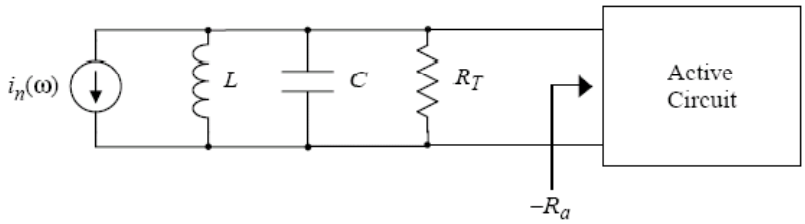


Fig. 6. One-port model of an LC oscillator.

Two ways to decrease phase noise are suggested by (2). First, we should use as few active devices as possible to minimize the number of noise sources in the oscillator. Second, the tank's magnitude response $|Z(\omega)|$ should be made as narrow as possible, i.e. a high quality factor (Q) should be employed for the LC-tank.

1.5.2 Two-Port View of Phase Noise

Returning to the two-port model shown in Figure 4, we now consider *f(s)* to be a parallel RLC tank as shown in Figure 7(a). The magnitude and phase responses of such a network are given in Figure 7 (b). As discussed before, we need zero degrees net phase shift around the feedback loop (any integer multiple of 360 degrees). Since noise sources in the oscillator circuit will cause temporary phase shifts in the feedback loop, the instantaneous oscillation frequency will be changing such that the tank produces a compensating phase shift, keeping the total phase shift around the loop equal to zero. Thus, phase noise can also be viewed as short-term instability in the frequency of oscillation [3].

The phase noise denoted by L{Δω}is defined as

$$L\{\Delta\omega\} = 10.\log\left[\frac{P_{1HZ}(\omega_0 + \Delta\omega)}{P_s}\right] \tag{3}$$

where, $P_{1Hz}(\omega_0 + \Delta\omega)$ represents the single sideband power measured in a 1-Hz bandwidth and located at a frequency offset Δω from the oscillation frequency ω_0. P_s represents the total signal power. A typical plot of L{Δω}is shown in Figure 8. Note the existence of regions of various slopes, as discussed in [1].

As mentioned above, to reduce the phase noise the magnitude response of the tank should be as sharp as possible, i.e. it should have a very narrow bandwidth or simply a high quality factor Q.

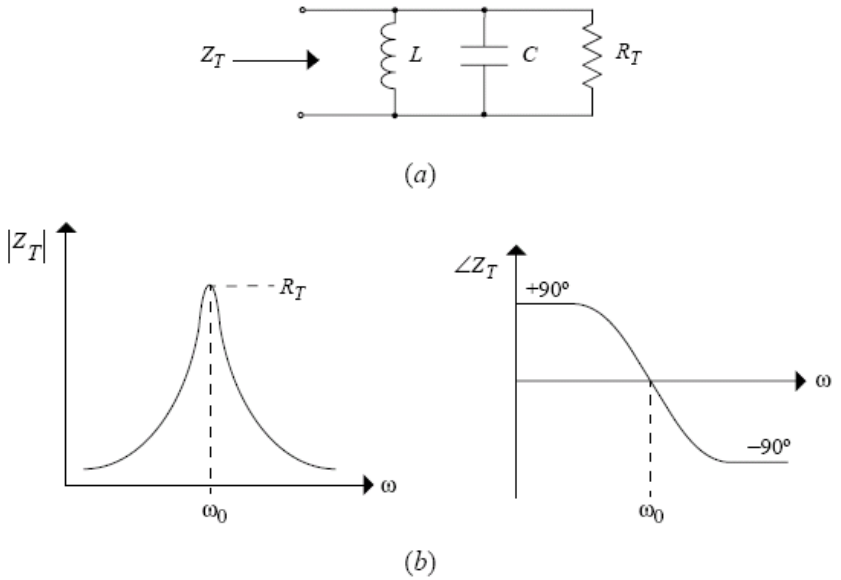


Fig. 7. (*a*) Parallel RLC tank. (*b*) Magnitude and phase response.

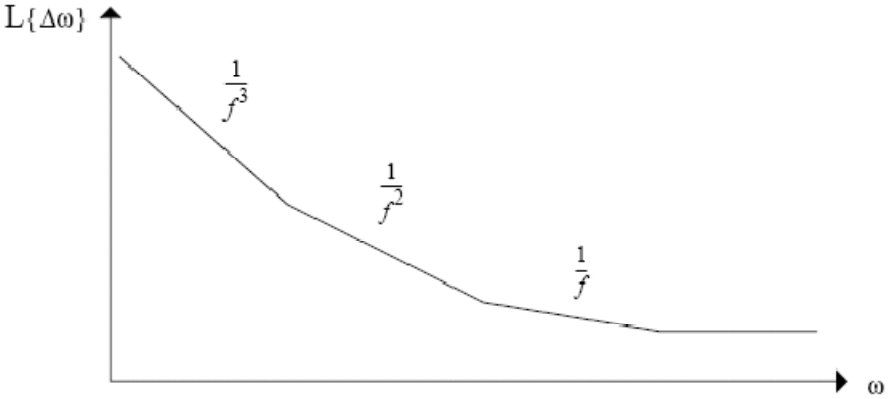


Fig. 8. General appearance of single-sideband phase noise.

I.5 Quality Factor

LC tanks, often referred as *LC* resonators, are represented as series or parallel *RLC* networks, since practical *LC* tanks contain additional resistive components. At resonance frequency, $\omega_0 = 1/\sqrt{LC}$, the tank impedance is purely resistive, and the phase of the impedance

response is exactly zero. At frequencies below (above) resonance, the tank impedance of the parallel RLC network is mainly inductive (capacitive). For series RLC networks, this scenario is exactly opposite.

The resonator's quality factor, Q, is generally defined as:

$$Q = \omega . \frac{Energy\ stored}{Average\ power\ dissipated} \tag{4}$$

The quality factor, which indicates the ability of the tank to retain energy, often determines the phase noise performance of LC VCOs. Also, Q indicates the steepness of the impedance near ω_0 or the sharpness of the peak impedance at ω_0. Therefore, Q can also be described by:

$$Q = \frac{\omega_0}{\Delta\omega_{-3dB}} \tag{5}$$

where, $\Delta\omega_{-3dB}$ is the −3dB bandwidth of the impedance response. Clearly, a larger Q results in a higher rejection of spectral energy away from the resonant frequency, leading to more purity of the oscillator output spectrum.

At resonance, the Q of the RLC networks is given by:

$$Q = \frac{R}{\omega_0 L} = \omega_0 RC \qquad (parallel\ RLC) \tag{6}$$

$$Q = \frac{\omega_0 L}{R} = \frac{1}{\omega_0 RC} \qquad (series\ RLC) \tag{7}$$

where, the dual nature of series and parallel RLC networks is apparent.

In wide-band VCOs, the equivalent tank impedance changes considerably along the tuning range. Figure 9 shows the simulated Q of a standard available on-chip inductor in a 0.18µm CMOS technology [2]. It is observed that the Q is linearly increased with the operation frequency. Aiming for a wideband VCO operating between 3– 6GHz, it is of interest to have the maximum Q at the highest frequencies, since the phase noise increases with frequency and may be reduced with the gain in Q. However, the variations in Q cause unwanted effects on the output amplitude. This issue will be explored in more detail in section 1.7.3.3.

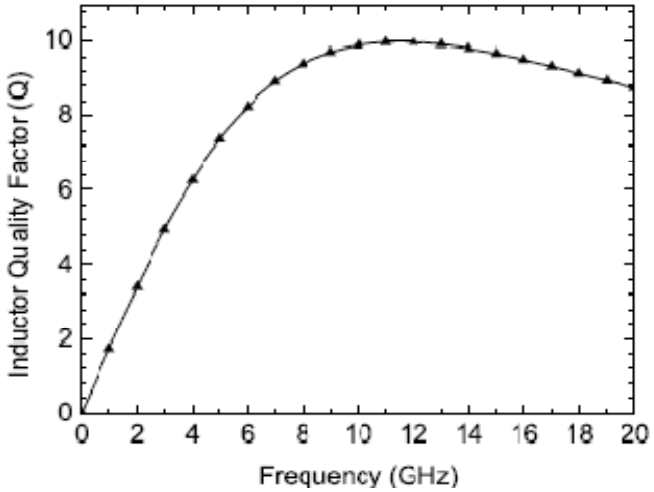


Fig. 9. Simulated Q for a circular 0.45nH on-chip inductor in a 0.18μm CMOS process [2].

1.6 Figure of Merit

Most oscillator designers usually report a figure of merit (FoM) value for their specific design. The most commonly used FoM in the RF community is the power-frequency-tuning-normalized (PFTN) figure of merit (FOM), as defined in [4, 6]:

$$FoM = 10.log\left(\frac{KT}{P}\left(\frac{\omega_{o,max}-\omega_{o,min}}{\Delta\omega}\right)\right) - L\{\Delta\omega\} \quad (8)$$

where, $\Delta\omega$ is the frequency offset from the carrier frequency ω_0, P is the power consumed by the VCO core, and $L\{\Delta\omega\}$ is the phase noise measured at an offset $\Delta\omega$ from the carrier. Also, $\omega_{0,max}$ and $\omega_{0,min}$ denote the high-side and the low-side frequencies of the tuning range, respectively.

1.7 Layout of Active and Passive Components

In CMOS VCO circuits, finding the optimal layout for both the passive and active devices is critical to achieving the best possible performance. One reason is the increasing impact of the parasitics in the device layout with technology scaling. Therefore, a well-optimized layout, which minimizes the parasitics and the noise sources, is very important. This section is devoted to these issues, including the integration of spiral inductors with high quality factor, active inductors, capacitors, varactor, resistors, and transistors for realizing the ultimate goal of VCO design.

1.7.1 Resistors

Figures of merit for resistors are sheet resistance, tolerance, parasitic capacitance, and voltage and temperature coefficients. In CMOS technology, resistors can be formed from the implanted well, the gate polysilicon, the source/drain active areas, and metal.

Polysilicon resistors are often used in integrated circuits for their low dependence on voltage and temperature. A low-doped p-type polysilicon resistor is used for applications

requiring high resistance. Despite its good parasitic capacitance, this resistor exhibits a 25% tolerance [8]. On the other hand, highly doped p-type polysilicon resistors are preferred in most cases because of their good matching and low parasitic.
Non-salicide high resistance poly has a sheet resistance between 800 - 1200 ohm/square. Non- salicide P+ (N+) poly resistance has a sheet resistance of 280-455 (95-180) ohm/square. These non-salicide poly resistors can be used for high-frequency circuits. Salicide P+/N+ poly resistance has a sheet resistance of 2-15 ohm/square, with small parasitic capacitance.

Diffusion resistors are similar to poly in terms of parasitic capacitance and voltage coefficient. They are typically controlled to a 10% tolerance. Salicide P+/N+ diffusion resistance has a sheet resistance of 2-15 ohm/square, with large parasitic. Non- salicide P+ (N+) diffusion has a sheet resistance of 110 -190 (60 -100) ohm/square. Non-salicide diffusion resistors are only suitable for low-frequency circuits, e.g. they are often used for ESD protection.

Well resistors have a large sheet resistance of 300 to 500 ohm/square, with large parasitic capacitance. Because of their strong dependence on voltage, they are usually used to feed a DC bias voltage.

Another high-performance resistor is formed of a thin metal film, further above the substrate in the wiring levels [9]. It has a sheet resistance of 0.025 to 0.115 ohm/square, with several attractive features such as low tolerance, low variation with voltage, and low parasitic.

1.7.2 Capacitors

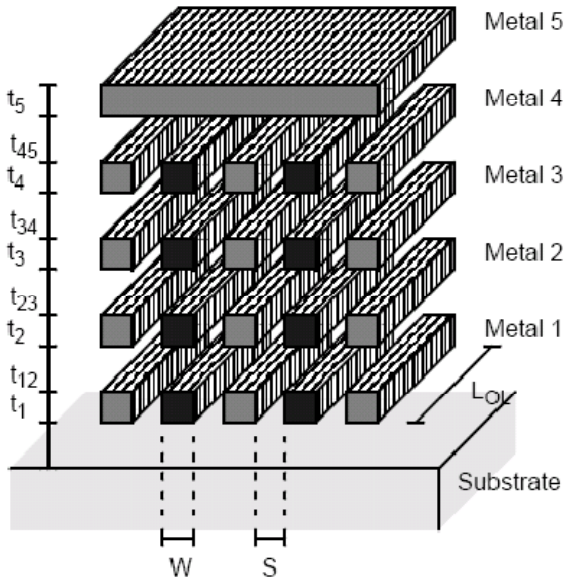


Fig. 10. Four Stacked Lateral Flux Capacitors. Fingers with dark cross-sections are connected to one port. The remaining fingers are connected to the other port [10].

Capacitors can be realized in any IC process using parallel plates from any two different layers (see Figure 10). Much larger capacitance per unit area can be obtained using the polysilicon layer as one or both of the capacitor plates. Nevertheless, a potential problem is that parasitic capacitance from the poly to the substrate may affect the circuit performance.
To achieve large capacitance per unit area, it is common to use several sandwiched-type capacitors and connect them in parallel (Figure 11). In order to obtain two capacitors with a good matching ratio, common-centroid and dummy devices are employed. Matched capacitors should have the same perimeter-area ratio.
Capacitors with relatively high-Q can also be implemented as interdigital, i.e. two conductors on the same plane are terminated in interdigitated fingers. These are used for low capacitance applications (0.05-0.5pF). With more metal layers available in a modern technology, the density of this capacitor tends to improve.

Since polysilicon-based capacitors are lossy, metal-insulator-metal (MIM) capacitors are preferred in RF design. MIM capacitors exhibit high density (e.g. 1-2fF/μm²) by using an ultra-thin layer of silicon nitride sandwiched along with an intermediate metal layer. Their typical Q exceeds 100 at 1GHz, with a relatively low parasitic capacitance (1% or less) [4].
MIM capacitors and Metal finger capacitors can be simply modeled by equivalent series RC networks, where R represents the series loss from the finite resistance of the metal plates.

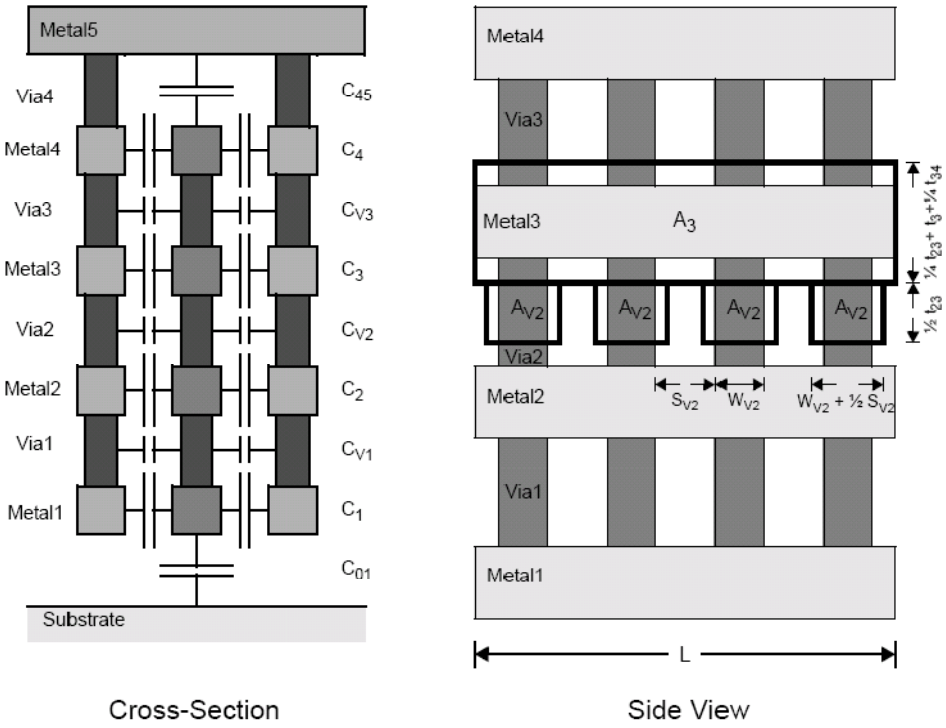


Fig. 11. Cross-Section of a Vertical Mesh Capacitor (left) and side view (right) [10].

1.7.3 Integrated Passive Inductors

On-chip inductor is by far the most critical component in an LC-tank oscillator, since its Q affects the phase noise performance and determines the power dissipation. As the process technology improves and the number of metal layers is increased, the quality (Q) of the passives is generally enhanced. Typical values of a standard on-chip inductor are in the range of a few nH with a Q ranging from 2-10 (for frequencies below 6GHz), depending on the technology and operating frequency [2].
On-chip inductors often need large loops and they have an area inefficient structure, compared to capacitors and resistors. However, planar inductors are widely implemented due to their flat Q and the ease of fabrication in standard processes. Typical on-chip spiral inductor structures are shown in Figure 12, which consist of multiple squares, octagonal, or circular spiraling turns forming its coils [4].

Making an inductor wider decreases the series resistance, and hence has a positive effect on Q at a particular frequency to a certain extent [12]. However, this would increase the coil capacitance and further reduce the resonant frequency. The maximal width of the metal (usually it is about 15-30 μm) is usually established using an optimization for resonance frequency or *Q*-factor.
The spiral is generally implemented in the topmost available metal layer because of its larger thickness than lower metal layers which helps reduce resistive losses. Also due to lower parasitic capacitance to the substrate, top metal layers give rise to higher self-resonance frequency. Note that the use of lower metal layers (closer to the substrate) brings down the self-resonance of the inductor. Sometimes two or more levels are connected in parallel to reduce resistance. Again, this technique effectively brings the coil closer to the substrate, which lowers its self-resonance.
The outer diameter of the inductor depends on how wide the inductor wire is, which in turn determines the area the inductor covers. For a given inductor area, one can fill in more turns until the entire space is occupied. Nevertheless, this is not recommended because of loss constraints and the fact that inner turns only slightly increase the overall inductance. Thus, spiral inductors are rarely filled to their maximum number of turns, and increasing the inductance is typically achieved by increasing the coil radius.

The inductance of a spiral is a complicated function of its geometry, and accurate computations require the use of field solvers. However, an approximate estimate, suitable for quick hand calculations as described in [12], gives the result which may deviate about 30% in comparison with field simulator results.

Square spirals offer the largest inductance per area compared to octagonal or circular spiral, whereas circular spirals is known to provide somewhat higher Q factor. The octagonal spirals are used as the next best alternative [4], since often circular geometries are not supported by many layout tools and not permitted in many technologies.

Another popular technique which provides a much more compact layout is to utilize a differential structure, as shown in Figure 13 [4], instead of using two single-ended inductors. In addition, the differential structure suppresses common- or even-mode capacitive parasitics and associated losses [14]. These benefits can also improve the self-resonance frequency and quality factor.

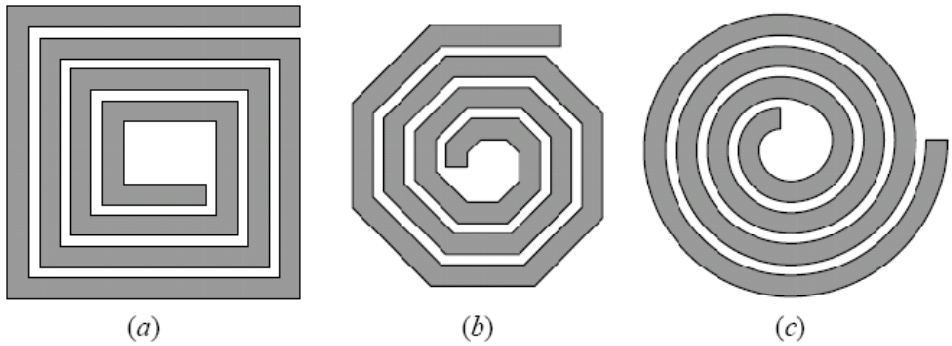


Fig. 12. Typical integrated inductors: (a) square, (b) octagonal, and (c) circular spirals [4].

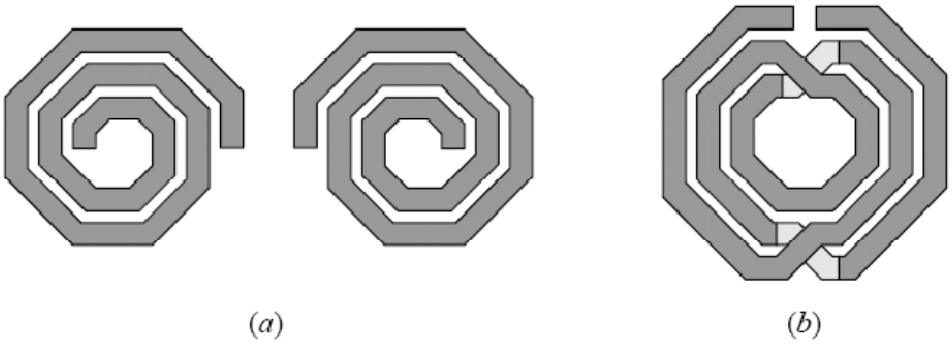


Fig. 13. A pair of single-ended inductors (a) and a differential inductor (b) with similar total inductance [4].

When two or more coils are used on the same chip, the distance between coil centers should be at least two times larger than the coil diameter for each couple of coils.

1.7.3.1 Measures for Q-enhancement

Three technological measures increasing *Q* are mentioned here. The first measure, which is anticipated to increase *Q* in two or three times, is using copper (Cu) alloys instead of aluminum (Al) alloys. The second measure is removal of the substrate under the coil (by etching or micromachining). It increases *Q* in addition by two or three times. The micromachined Cu inductors may have *Q*'s as high as 50, and allow realization of bandpass filters with the insertion loss which is better than –5dB at the frequency about 6GHz.

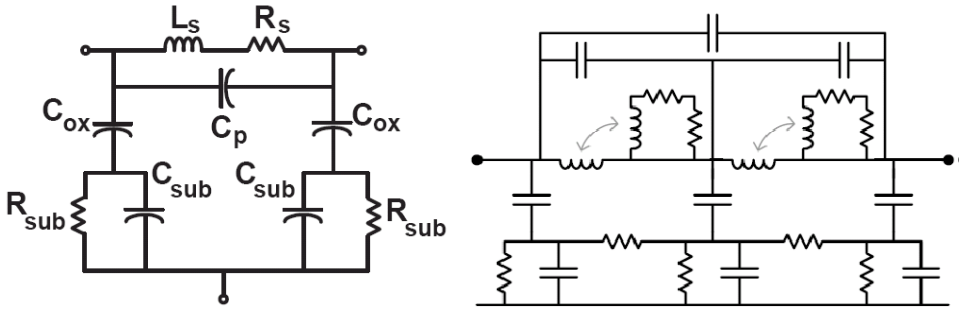
Third measure is a pattern ground-shield, which has been shown to improve the Q of the inductor, since it reduces the capacitive coupling to the lossy substrate [13]. This technique also reduces the noise coupled from the substrate at the penalty of reduction of the self resonant frequency of the inductor.

Today, such inductors are common in standard available design kits provided by the manufacturers. However, despite these efforts, the inductor Q is still one of the main uncertain parameters in RF circuit design and in many cases the major bottleneck of entire systems.

1.7.3.2 Inductor Modeling

The area of an on-chip inductor can span up to hundreds of μm across and does not scale down with the technology [2]. Aside from their large physical dimensions, integrated inductors are usually described by simple lumped equivalent networks.

Figure 14 (a) shows a lumped π-model for an integrated inductor. L_s describes the series inductance and R_s represents the series resistance of the metal layer. C_p models the interwinding capacitance between the traces. In silicon technology the fairly conductive substrate is close to the spiral, which is essentially creating a parallel plate capacitor (C_{ox}) that resonates with the inductor. R_{sub} model the resistive path in the substrate which also reduces the Q of the inductor. C_{sub} models the capacitive coupling from metal to substrate which reduces the resonant frequency of the inductor.



(a) (b)

Fig. 14. (a) Basic π-model of an integrated inductor (b) wideband lumped equivalent.

The π-equivalent network is a narrowband model only valid in the close vicinity of that particular frequency and is not suitable in wideband designs [4].

The network shown in Figure 14 (b) approximates the frequency dependence of the most important characteristics of the coil using an expanded lumped equivalent network. As a result, its validity holds over a much wider frequency range and it is better suited for wideband design analysis [4].

1.7.3.3 Effect of frequency

The Q value of ideal inductors is improved with the increase in frequency. This is however not the case for on-chip inductors because the parasitic capacitance and substrate losses show their significance at higher frequencies [12].

The series dc resistance of the inductor is the dominant loss contributor at low frequencies (<1GHz). At higher frequencies, the series resistance rises considerably, due to skin and proximity effects. The skin effect forces the current in the inductor to flow on the outside of the spiral. This makes the inner turns of the spiral less effective than the outer turns and the effective series resistance is increased.

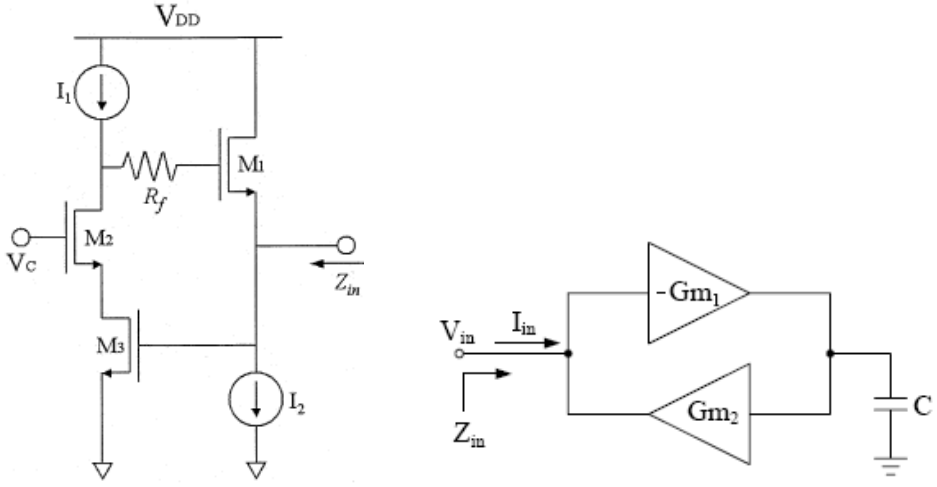
Proximity effects due to fields from adjacent turns result in a similar frequency-dependent non-uniform current distribution and corresponding loss increase. Also, the flow of currents in the substrate translates to additional losses which are a strong function of the substrate resistivity and become significant as frequency increases.

As a result, Q initially rises linearly with frequency since the loss is dominated by the coil's dc series resistance. Eventually, skin and proximity effects as well as substrate losses become dominant. Thus, Q gradually peaks to a maximal value, and beyond which it experiences a fast decline as frequency approaches the coil's self-resonance. Note that the impact of the above effects on the inductor performance is very complicated, and therefore, software tools must be used for its performance optimization.

1.7.4 Active Inductor Design

Active inductors may often be of interest in RF circuits, since passive inductors are not economical in terms of the fabrication technology and die area. An active inductor can be realized by connecting two transconductors with resistive feedback (R_f), as shown in Figure 15 (a) [15-18]. This realization is based on the gyrator-C topology (Figure 15(b)). In Figure 15(a), transistor M2 is employed to reduce the output conductance (g_{ds}), as a result of which the inductance, quality factor, and frequency tuning range are improved. Also, the feedback resistance R_f between M_1 and M_3 significantly increases the inductance [16]. The resistance (R_f) is usually implemented by a passive poly layer.

Due to low-inductance value and narrow frequency range of the above topology, improved cascode structure employing active resistors in the feedback line is also proposed [19]. The fully tunable active inductor (TAI) and its equivalent circuit model are shown in Figure 16(a) and Figure 16(b), respectively. This active inductor exploits a tunable feedback resistance, implemented by connecting the resistor (R_f) in parallel with a transistor. The gate-source voltage (V_{tune}) in this transistor controls the total effective resistance (R_{eff}). This reduces the output conductance and improves the quality factor.



(a) (b)

Fig. 15. (a) Schematic of cascode-grounded active inductor with a feedback resistance (b) Gyrator topology

The equivalent capacitance, inductance, and resistors are [19]:

$$C_{eq} = C_{gs3} \tag{9}$$

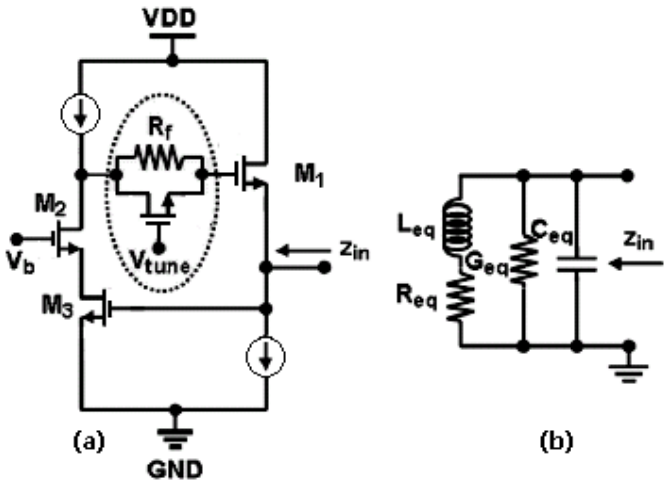


Fig. 16. (a) TAI topology (b) Equivalent circuit model of active inductor

$$L_{eq} = \frac{g_{m1}g_{m2}C_{gs1} + \omega^2 C_{gs1}^2 C_{gs2}(R_f g_{ds2} + 1)}{g_{m1}^2 g_{m3} g_{m3} + \omega^2 g_{m2} g_{m3} C_{gs1}^2} \tag{10}$$

$$R_{eq} = \frac{g_{m1}g_{ds2}g_{ds3} + \omega^2\left[g_{m2}C_{gs1}^2 - g_{m1}C_{gs1}C_{gs2}(R_f g_{ds2} + 1)\right]}{g_{m1}^2 g_{m2} g_{m3} + \omega^2 g_{m2} g_{m3} C_{gs1}^2} \tag{11}$$

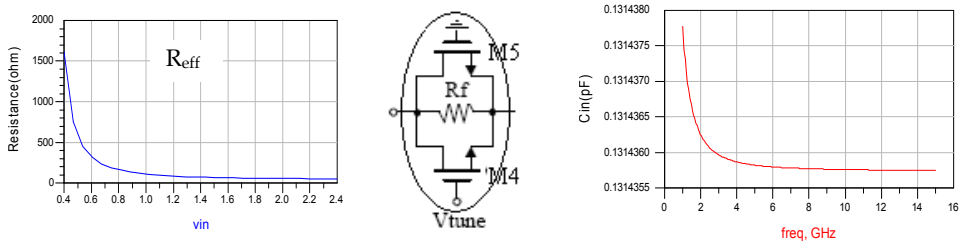
$$G_{eq} = \frac{2g_{ds2} + R_f g_{ds2}^2}{R_f g_{ds2} + 1} \tag{12}$$

In (12), the effect of feedback resistor is shown by $(R_f g_{ds2} + 1)$, which is designed for a value greater than unity. Decreasing R_{eq} by the help of R_f results in an increase in L_{eq}. The quality factor and the input impedance of TAI can be obtained from [15]:

$$Q = \left(\frac{\omega L_{eq}}{R_{eq}} \right) \left[\frac{1 - (R_{eq}^2 C_{eq}/L_{eq}) - \omega^2 L_{eq} C_{eq}}{1 + R_{eq} G_{eq} \{1 + (\omega L_{eq}/R_{eq})^2\}} \right] \tag{13}$$

$$z_{in} = \left[\frac{R_{eq} + j\omega L_{eq}}{(1 + R_{eq} G_{eq} - \omega^2 L_{eq} C_{eq}) + j\omega (R_{eq} C_{eq} + L_{eq} G_{eq})} \right] \tag{14}$$

Clearly, with decreasing R_{eq}, the quality factor is improved.
Note that in conventional TAI topology, V_b=constant (see Figure 16 (a)). As can be seen from equations (10), (11), and (13), active resistor has direct effect on increasing L_{eq} and R_{eq}. However, this increase in R_{eq} will degrade the quality factor. To overcome this problem, V_b can be utilized as the extra tuning voltage to control the g_{ds} of transistor M2. Thus, the required inductance and quality factor are achieved by controlling V_{tune} and V_b simultaneously.
For further enhancement of quality factor and inductance, one can utilize the transistor M5 in parallel with feedback resistance R_f, as shown in Figure 17(b) [18]. This transistor, which operates in the cut-off region, exhibits a frequency dependent capacitance as shown in Figure 17(c).
Using a 0.13μm CMOS technology, a tunable resistance from 100Ω to 1.6 kΩ may be achieved [18] for V_{tune}=1.2V to V_{tune}=0.4V, as illustrated in Figure 17(a).



(a) (b) (c)

Fig. 17. (a) Variation of effective resistance versus tuning voltages (b) Proposed active resistance with parallel MOSFET (c) Variation of capacitance in proposed active resistance versus frequency.

The values of each component of equivalent circuit model are expressed below (Cp is equivalent capacitance of M5):

$$C_{eq} = C_{gs3} - \frac{2\omega C_p R_{eff} g_{ds2} \left(R_{eff} g_{ds2} + 1 \right) - R_{eff} \omega C_p \left(R_{eff} g_{ds2}^2 + 2 g_{ds2} \right)}{\left(R_{eff} g_{ds2} + 1 \right)^2 + \omega^2 C_p^2 R_{eff}^2} \tag{15}$$

$$G_{eq} = \frac{2\omega^2 C_p{}^2 R_{eff}{}^2 g_{ds2} + \left(R_{eff} g_{ds2} + 1\right)\left(R_{eff} g_{ds2}{}^2 + 2g_{ds2}\right)}{\left(R_{eff} g_{ds2} + 1\right)^2 + \omega^2 C_p{}^2 R_{eff}{}^2} \tag{16}$$

$$R_{eq} = \frac{g_{m1}g_{ds2}g_{ds3} + \omega^2\left[g_{m2}C_{gs1}{}^2 + \left(C_{gs1}C_{gs2}\right)\left[\frac{g_{m1}C_pC_{gs1}R_{eff}{}^2 g_{ds2}}{1+\omega^2 C_p{}^2 R_{eff}{}^2} - g_{m1}\left(1+\frac{R_{eff}g_{ds2}}{1+\omega^2 C_p{}^2 R_{eff}{}^2}\right)\right]\right]}{g_{m1}{}^2 g_{m2}g_{m3} + \omega^2 g_{m2}g_{m3}C_{gs1}{}^2} \tag{17}$$

$$L_{eq} = \frac{g_{m1}g_{m2}C_{gs1} + \omega^2\left(C_{gs1}C_{gs2}\right)\left[\frac{g_{m1}C_pR_{eff}{}^2 g_{ds2}}{1+\omega^2 C_p{}^2 R_{eff}{}^2} + g_{m1}C_{gs1}\left(1+\frac{R_{eff}g_{ds2}}{1+\omega^2 C_p{}^2 R_{eff}{}^2}\right)\right]}{g_{m1}{}^2 g_{m2}g_{m3} + \omega^2 g_{m2}g_{m3}C_{gs1}{}^2} \tag{18}$$

In order to have L_{eq} greater and R_{eq} smaller than other conventional inductors, the following relations should be satisfied.

$$C_p > \frac{-g_{ds2}}{\omega^2 C_{gs1}} \tag{19}$$

$$C_p > \frac{C_{gs1}g_{ds2}}{\omega^2} \tag{20}$$

1.7.5 Varactors

Varactors are essential elements of voltage-controlled oscillators (VCOs). The key figures of merit for varactors are tunability (C_{max}/C_{min}), CV linearity for VCO gain variation, quality factor Q, tolerance, and capacitance density [8].

In general, two types of varactors have been developed for the RF CMOS processes, MOS accumulation mode capacitor (MOS varactor) and CMOS diode.

CMOS diode varactors are basically reverse-biased p-n junctions which can be implemented using the available p+/n-diffusions and n- or p-wells [4]. These varactors exhibit tunability of about 1.7:1 over a 3-V range, and can be used where fine tuning of capacitance is required. Also, they provide better linearity than MOS varactors.

The MOS varactor can be realized with an *n*-channel MOSFET fabricated in an n-well. Its main advantage is the high intrinsic C_{max}/C_{min} that is much higher than that of p-n junction varactors. This provides an excellent tunability over a wide frequency range and sufficiently high Q factor. The performance of this varactor improves with technology scaling.

Also, a hyper-abrupt (HA) junction varactor has been reported in the literature with a nearly linear *C–V* tuning ratio of 3.1 and a *Q* exceeding 100 at 2 GHz [8].