The Switched Mode Power Amplifiers

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1. Introduction

The power amplifier (PA) is a key element in transmitter systems, aimed to increase the power level of the signal at its input up to a predefined level required for the transmission purposes. The PA's features are mainly related to the absolute output power levels achievable, together with highest efficiency and linearity behaviour.
From the energetic point of view a PA acts as a device converting supplied dc power (P_{dc}) into microwave power (P_{out}). Therefore, it is obvious that highest efficiency levels become mandatory to reduce such dc power consumption. On the other hand, a linear behaviour is clearly necessary to avoid the corruption of the transmitted signal information. Unfortunately, efficiency and linearity are contrasting requirements, forcing the designer to a suitable trade-off.
In general, the design of a PA is related to the operating frequency and application requirements, as well as to the available device technology, often resulting in an exciting challenge for PA designers, since not an unique approach is available.
In fact, PAs are employed in a broad range of systems, whose differences are typically reflected back into the technologies adopted for PAs active modules realisation. Moreover, from the designer perspective, to improve PAs efficiency the active devices employed are usually driven into saturation. It implies that a PA has to be considered a non-linear system component, thus requiring dedicated non linear design methodologies to attain the highest available performance.
Nevertheless, for high frequency applications it is possible to identify two main classes of PA design methodologies: the trans-conductance based amplifiers with Harmonic Tuning terminations (HT) (Colantonio et al., 2009) or the Switching-Mode (SM) amplifiers (Grebennikov & Sokal, 2007; Krauss et al., 1980). In the former, the active device acts as a nonlinear current source controlled by the input signal (voltage or current for FET or BJT devices respectively). A simplest schematic view of such an amplifier for FET is reported in Fig. 1a. Under this assumption, the high efficiency condition is achieved exploiting the device nonlinear behaviour through a suitable selection of both input and output harmonic terminations. More in general, the trans-conductance based amplifiers are identified also as Class A, AB, B to C considering the quiescent active device bias points, resulting in different output current conduction angles from 2π to 0 respectively.
The most famous solution of HT PA is the Class F approach (Gao, 2006; Colantonio et al, 2009), while for high frequency applications and taking into account practical limitations on

the control of harmonic impedances, several solutions have been successfully proposed (Colantonio et al., 2003).
Conversely, in the SM PA, the active device is driven by a very large input signal to act as a ON/OFF switch with the aim to maximise the conversion efficiency reducing the power dissipated in the active devices also. A schematic representation of a SM amplifier is depicted in Fig. 1b. When the active device is turned on, the voltage across its terminals is close to zero and high current is flowing through it. Therefore, in this part of the period the transistor acts as a very low resistance, ideally short circuit (switch closed) minimising the overlap between the current and voltage waveforms. In the other part of the period, the active device is turned off acting as an open circuit. Therefore, the current is theoretically zero while high voltage is present at the device terminals, once again minimising the overlap between voltage and current waveforms. If the active device shows a zero on resistance and an infinite off resistance, a 100% efficiency is theoretically achieved. The latter is of course an advantage over Class A or B, where the maximum theoretical efficiencies are 50 % and 78 % respectively. On the other hand, Class C could achieve high efficiency levels, despite a significant reduction in the maximum output power level achievable (theoretically 100% of efficiency for zero output power). Nevertheless, the HT PAs are intrinsically able to amplify the input signal with higher fidelity, since the active device is basically represented by a controlled current source (FET case) whose output current is directly related to the input voltage. Instead, in SM PAs the active device is assumed to be ideally driven in the ON and OFF states, thus exhibiting a higher nonlinear behaviour. However, this characteristic does not represent a trouble when signals with constant-envelope modulation are adopted.
On the basis of their operating principle, SM amplifiers are often considered as DC to RF converter rather than RF amplifiers.

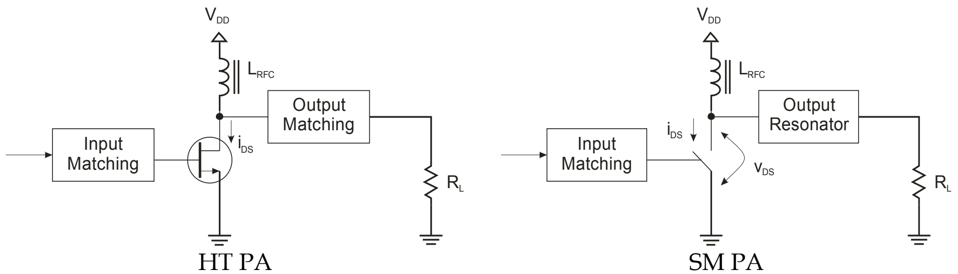


Fig. 1. Simplified view of a simple single ended HT (left) and SM (right) PA.

Different SM PA classes of operation have been proposed over the years, namely Class D, S, J, F^{-1} (Cripps, 2002; Kazimierczuk, 2008), while the most famous and adopted is the Class E PA (Sokal & Sokal, 1975; Sokal, 2001) that will be described in deep detail in the following. As will be shown, these classes are based on the same operating principle while their main differences are related to their circuit implementation and current-voltage wave shaping only.
The applications of SM PAs principles have initially been limited to amplifiers at lower frequencies in the megahertz range, due to the active device and package parasitics practically limiting the operating frequencies (Kazimierczuk, 2008). They have also been

applied to DC/DC power converters that also operate at lower switch frequencies (Jozwik & Kazimierczuk, 1990; Kazimierczuk & Jozwik, 1990). Recently, their principles of operation have been extended and applied to RF and microwave amplifier design, made possible by the high-performance active devices nowadays available based on silicon (Si), gallium arsenide (GaAs), silicon germanium (SiGe), silicon carbide (SiC), and gallium nitride (GaN) technologies (Lai, 2009).

2. Switching mode generic operating principle

The operating principle of every SM PA is based on the idea that the active device operates in saturation, thus it can be represented as a switch and either voltage or current waveforms across it are alternatively minimized to reduce overlap, so minimizing power dissipation in the device itself. If the transistor is an ideal switch, a 100% of efficiency can be achieved by the proper design of the output matching network. As reported in Fig. 1b, the output resonator can be assumed, in the simplest way, as an ideal *L-C* series resonator at fundamental frequency, terminated on a series load resistance (R_L). The role of the resonator is to shape the voltage and current waveforms across the switch in order to avoid power dissipation at higher harmonics. In fact, an ideal *L-C* series resonator shows zero impedance at resonating frequency ($\omega_0=(LC)^{-1/2}$) and infinite impedance for every $\omega\neq\omega_0$. It follows that fundamental current only is flowing into the output load and fundamental voltage only is generated at its terminals. Consequently, 100% of efficiency is obtained (being zeroed the overlap between voltage and current waveforms over the transistor, thus being nulled the power dissipated in it) and no power is delivered at harmonic frequencies in the load, being the latter not allowed to flow into the load R_L.

In actual cases, several losses mechanisms, such as ohmic and capacitive discharge or leakage, cause an unavoidable overlapping between the voltage and current waveforms, together with power dissipation at higher harmonics, thus limiting the maximum achievable efficiency levels.

The most relevant losses in SM PA are represented by:

- parasitic capacitors, such as the device drain to source capacitance C_{ds}. The presence of such capacitance causes a low pass filter behaviour at the output of the active device, affecting the voltage wave shaping with a consequent degradation in the attainable power and efficiency levels. In fact, considering the active device as the parallel connection of a perfect switch and the parasitic capacitance C_{ds}, the higher voltage harmonics are practically shorted by C_{ds} and only few harmonics can be reasonably controlled by the loading network.
- parasitic resistance, such as the drain-to-source resistance when the transistor is conducting R_{ON} (ON state). In fact, due to the non zero resistance when the switch is closed, a relevant amount of active power will be dissipated in the transistor causing a lowering in the achievable efficiency.
- non-zero transition time, due to the presence of parasitic effects, which increase the voltage and current overlap.
- implementation losses due to the components (distributed or lumped elements) employed to realise the required input and output matching networks.

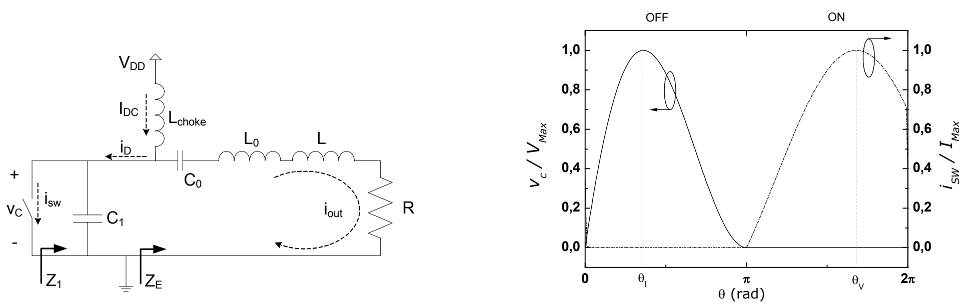
The entity of the parasitic components as well as the associated losses are strictly related to the characteristics of the active device used, especially when designing RF PA (Kazimierczuk, 2008; Lai, 2008).

3. The Class E Amplifier

Firstly presented in the early 70's in (Sokal & Sokal, 1975), the Class E power amplifier recently received more attention by microwave engineers with the growing demand of high efficient transmitters in wireless communication systems.
It has been widely adopted in constant envelope based communication systems, but represents a valid alternative if combined with envelope varying technique also, like envelope elimination and restoration or Chireix's outphasing technique (Cripps, 2002).
A complete analysis of the Class E amplifier is herein presented, making the assumption of a very idealized active device switching action. The topology considered is the most common one, firstly presented in (Sokal & Sokal, 1975), although different Class E topologies have been conceived and studied during the past (Mader et al., 1998; Grebennikov, 2003; Suetsugu & Kazimierczuk, 2005). In order to clarify Class E operation, a real device-based design is also briefly presented.

3.1 Analysis with a generic duty cycle

The basic topology of a single ended Class E power amplifier is depicted in Fig. 2. The active device is schematically represented as an ideal switch and it is shunted by the capacitance C_1, which include the output equivalent capacitance of the active device also. The output network is composed by an ideal filter C_0-L_0 with a series R-L impedance.



(a) (b)

Fig. 2. Basic topology of a Class E amplifier (a) corresponding ideal waveforms (b).

Such a circuit is usually analyzed in time domain, which is a straightforward but tedious process, requiring the solution of non linear differential equations. Anyway, some hypotheses can be adopted to carry out a simplified analysis useful to understand the underling operating principle.
Considering the series resonator C_0-L_0 to behave as an ideal filter, i.e. with an infinite (or high enough) Q factor, harmonics and all frequency components different from the fundamental frequency can be considered as filtered out and do not play any role in the

solution of the system. As a consequence, the current flowing into the output branch of the circuit can be assumed as a pure sinusoidal, with its own amplitude I_M and its phase ϕ (Raab, 2001):

$$i_{out} = I_M \cdot \sin(\theta + \phi) \tag{1}$$

Where $\theta = \omega \cdot t$.

Consequently, from Kirchhoff laws the current i_D (see Fig. 2), which flows entirely through the switch during the ON period (i_{SW}) or entirely through the capacitance C_1 during the OFF period, can be written as:

$$i_D = I_{DC} - I_M \cdot \sin(\theta + \phi) \tag{2}$$

Assuming for simplicity a 50% of duty cycle (the analysis for a generic duty cycle is available in (Suetsugu & Kazimierczuk, 2007)), the current flowing into the switch i_{SW} can be expressed as:

$$i_{sw}(\theta) = \begin{cases} 0, & 0 \le \theta \le \pi \\ I_{DC} - I_M \cdot \sin(\theta + \phi), & \pi \le \theta \le 2\pi \end{cases} \tag{3}$$

And analogously the current in the capacitor C_1 becomes:

$$i_C(\theta) = \begin{cases} I_{DC} - I_M \cdot \sin(\theta + \phi), & 0 \le \theta \le \pi \\ 0, & \pi \le \theta \le 2\pi \end{cases} \tag{4}$$

While the voltage across the capacitance v_C can be easily inferred by integration of (4), resulting in the following expression:

$$v_C(\theta) = \begin{cases} \dfrac{1}{\omega \cdot C_1} \cdot \left(I_{DC}\theta + I_M \cdot \cos(\theta + \phi) - I_M \cdot \cos(\phi)\right), & 0 \le \theta \le \pi \\ 0, & \pi \le \theta \le 2\pi \end{cases} \tag{5}$$

The resulting theoretical current and voltage waveforms are depicted in Fig. 2b.

It can be noted that current and voltage across the switch do not overlap, thus no power dissipation exists on the active device. The unique dissipative element in the circuit is the loading resistance R, which is active at fundamental frequency only. Then, from these assumption it follows that the DC to RF power conversion happens without losses and the theoretical efficiency is 100%.

The quantities I_{DC}, I_M and ϕ have still to be determined as functions of maximum current and voltage allowed by the adopted active device, I_{Max} and V_{Max} respectively, and of operating angular frequency ω.

For this purpose, it has to note that the capacitance C_1 should be completely discharged at the switching turn on, which implies that the voltage v_C has to be null in correspondence of the instant π (see Fig. 2b):

$$v_C(\theta)\Big|_{\theta=\pi} = 0 \tag{6}$$

Such condition is usually referred as Zero Voltage Switching (ZVS) condition, which implies that the capacitance C_1 should not be short circuited by the switch turn on when its voltage is still high (Sokal & Sokal, 1975).
The second condition, namely Zero Voltage Derivative Switching (ZVDS) condition, or soft-switching condition, implies that the current starts to flow from zero after the switch turn on and then increases gradually, in order to prevent worsening in circuit performance due to mistuning of the waveforms (Sokal & Sokal, 1975). This condition is written as:

$$i_C(\theta)\Big|_{\theta=\pi} = \frac{d}{d\theta} v_C(\theta)\Big|_{\theta=\pi} = 0 \tag{7}$$

Substituting (4) in the previous equations, from (6) it follows:

$$I_{DC} \cdot \pi - 2 \cdot I_M \cos(\phi) = 0 \tag{8}$$

While from (7) it follows:

$$I_{DC} + I_M \cdot \sin(\phi) = 0 \tag{9}$$

Thus the following relationships can be inferred:

$$\tan(\phi) = -\frac{2}{\pi} \tag{10}$$

$$\frac{I_{DC}}{I_M} = -\sin(\phi) = \frac{2}{\pi} \cdot \cos(\phi) \tag{11}$$

The maximum current flowing into the switch is given by:

$$I_{Max} = I_{DC} + I_M \tag{12}$$

And it occurs in correspondence of the angle

$$\theta_I = \frac{3}{2} \cdot \pi - \phi \tag{13}$$

Similarly, for the voltage across the switch its maximum value occurs in correspondence of the angle θ_V (see Fig. 2b), which can be inferred nulling the derivate of v_c given by (5).
Thus, accounting for (11), it follows:

$$\theta_V = -2 \cdot \phi \tag{14}$$

and

$$V_{Max} = -2 \cdot \phi \cdot \frac{I_{DC}}{\omega C_1} \tag{15}$$

However, the value of the capacitance C_1 is still an unknown variable. It appears in the definition of the voltage waveform, and it is convenient to use voltage constraints in order to obtain its expression. In fact, its average value must be equal to the supplied DC voltage V_{DD}; thus it follows:

$$V_{DD} = \frac{1}{2\pi} \int_0^{\pi} v_C(\theta)\, d\theta \tag{16}$$

Which solved lead to:

$$V_{DD} = \frac{1}{2\pi} \cdot \frac{1}{\omega \cdot C_1} \cdot \left(I_{DC} \cdot \frac{\pi^2}{2} + 2 \cdot I_M \sin(\phi) - I_M \cdot \pi \cdot \cos(\phi) \right) \tag{17}$$

from which the value of C_1 can be finally determined remembering (11)

$$C_1 = \frac{I_{DC}}{\pi \cdot \omega \cdot V_{DD}} \tag{18}$$

This also suggests a simple relationship between DC current and bias voltage.
At this point, waveforms in Fig. 2b have been completely determined in the time domain, without recurring to the frequency domain. However, the remaining elements of the circuit, DC power, output power and output impedance have still to be determined.
As stated before, all the DC power is converted to RF power and dissipated into the load resistance at fundamental frequency:

$$P_{DC} = I_{DC} \cdot V_{DD} = \frac{1}{2} \cdot I_M \cdot V_M = P_{RF} \tag{19}$$

where V_M is the amplitude of fundamental component of the voltage across R which can be obtained by (19) and replacing (11):

$$V_M = 2 \cdot \frac{V_{DD} \cdot I_{DC}}{I_M} = -2 \cdot V_{DD} \cdot \sin(\phi) \tag{20}$$

The value of the resistance R is simply obtained as the ratio between V_M and I_M:

$$R = \frac{V_M}{I_M} = 2 \cdot \frac{V_{DD}}{I_{DC}} \cdot \sin(\phi)^2 \tag{21}$$

Clearly, if a standard 50 Ohm termination is required, an impedance transformer is necessary to adapt such load to the required R value.
Finally, the inductance L is computed taking into account that its reactive energy is exchanged, at every cycle, with the capacitance C_1. Thus it follows:

$$\frac{1}{2\cdot\pi}\cdot\frac{1}{\omega C_1}\int_0^{\pi}\left[I_{DC}-I_M\cdot\sin\left(\theta+\phi\right)\right]^2 d\theta=\frac{1}{2}\cdot\omega\cdot L\cdot I_M{}^2 \tag{22}$$

where the expression in the integral represents the voltage across the capacitance C_1 during the OFF period. The value for the inductance L is therefore given by:

$$L=\frac{1}{\omega\cdot C_1}\cdot\left(\frac{\pi}{2}-\frac{4}{\pi}\cdot\cos\left(\phi\right)^2\right) \tag{23}$$

Alternatively, R and L can be found by calculation off in-phase and quadrature voltage components, as elsewhere reported (Mader et al., 1998; Cripps, 1999).
The series impedance R-L can be put together in order to obtain a more compact and useful expression for the output branch impedance (Mader et al., 1998) normalized to the shunt capacitance C_1:

$$Z_E=\frac{0.28}{\omega C_1}\cdot e^{j49°} \tag{24}$$

With reference to Fig. 2, the impedance Z_1 seen by the ideal switch is obtained by the shunt connection of the capacitance C_1 and Z_E and is herein given in its simplified formulation (Colantonio et al., 2005):

$$Z_1=\frac{0.35}{\omega C_1}\cdot e^{j36°} \tag{25}$$

Remaining reactive components, L_0 and C_0, are easily calculated by means of:

$$\omega^2=\frac{1}{L_0\cdot C_0} \tag{26}$$

Provided a high enough Q factor, the values of L_0 and C_0 are non uniquely defined and any pair of resonant element can be used.
The analysis performed here was intended for the most common case of 50% duty cycle (i.e. π conduction angle). In this case the relations are greatly simplified thanks to the properties of trigonometric functions. However, Class E approach is possible for any value of duty cycle: a detailed analysis can be found in (Suetsugu & Kazimierczuk, 2007; Colantonio et al., 2009) where all electrical properties and component values are evaluated as a function of duty cycle. It can be demonstrated that under ideal assumption the maximum output power does not occur in correspondence of a 0.5 duty cycle, but for a slightly higher value (0.511). Anyway, in terms of output power capability, this increment is extremely low (about 1‰) and a standard 0.5 duty cycle could be assumed in the design, unless differently required.

3.2 A Class E design example

In order to illustrate the application of the relations obtained in the analysis, a simple Class E design example is described, based on an actual active device, specifically a GaAs pHEMT.

The device exhibits a breakdown voltage of about 25 V and a maximum output current of 400 mA. From S-parameter simulation, an output capacitance of 0.35pF results at 2.5 GHz, the selected operating frequency. Considering this capacitance as the minimum value for the shunt capacitance C_1, the network elements can be easily calculated through the previous relationships.
From (20) and taking into account the maximum voltage, the bias voltage is set to V_{DD}=6V. Hence, from the inversion of (18), the DC component of drain current is determined, resulting in I_{DC}=105 mA.
At this point, using (21) and (23) or, alternatively, equation (24), the values of output matching network are R=33Ω and L=1.67 nH. If considering a standard output impedance of 50Ω, a transforming stage is necessary.

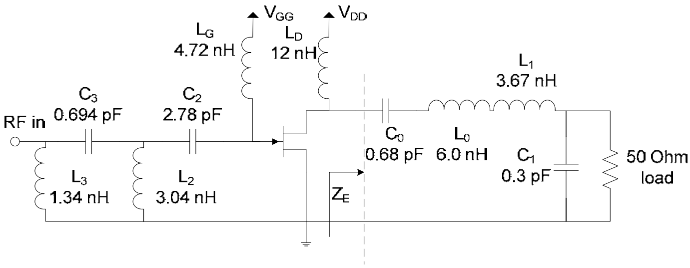


Fig. 3. Schematic of a 2.5GHz GaAs HEMT Class E amplifier.

Standing the value of optimum load, the impedance matching can be easily accomplished by a single L-C cell. A series inductance - parallel capacitance configuration has been chosen.
Lumped elements for the filtering output network have then determined, selecting an inductance L_0=6nH and a resulting capacitance C_0=0.68pF. The complete amplifier schematic is depicted in Fig. 3, while the simulated output power, gain and efficiency versus input power are shown in Fig. 4.

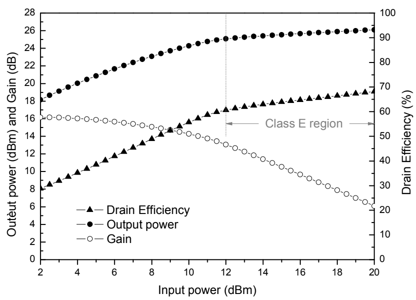
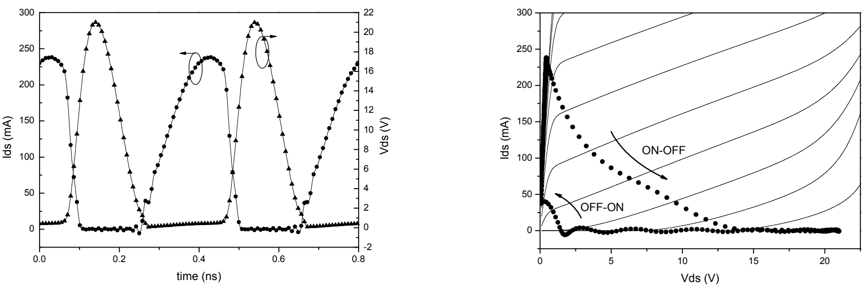


Fig. 4. Simulated performance of the 2.5GHz Class E amplifier.

It is worth to notice that, under a continuous wave excitation, Class E behavior is achieved only at a certain level of compression, i.e. when the large input sinusoidal waveform implies a “square-shaping” effect on the output current, due to active device physical limits, thus approaching a switching behavior. The output current and voltage waveforms and load line are reported in Fig. 5, showing a good agreement with the theoretical expected behavior (compare with ideal waveforms depicted in Fig. 2b).



(a) (b)

Fig. 5. Output current and voltage waveforms (a) and load line (b) of the 2.5GHz Class E amplifier.

3.3 Drawbacks

As already outlined, Class E power amplifiers have some practical limitations, mainly due to their maximum operating frequency. Such limitations are partially related to the cut-off frequency of the active device, while are mainly due to the circuit topology and switching operation. In fact, as reported in (Mader et al., 1998), a Class E maximum frequency can be approximated by:

$$f_{Max} = \frac{I_{DS}}{2\pi^2 \cdot C_1 \cdot V_{DD}} \simeq \frac{I_{Max}}{56.5 \cdot C_1 \cdot V_{DD}} \tag{27}$$

Practically the lower limit of C_1 is given by the active device output capacitance C_{ds}. Consequently, the value of maximum operating frequency strongly depends on the device adopted for the design, on its size and then on the maximum current it can handle. For RF and microwave devices, the maximum frequency in Class E operation is generally included between hundred of megahertz (for MOS devices) and few gigahertz (for small MESFET or pHEMT transistors).

Additionally, at microwave frequencies higher order voltage harmonic components can be considered as practically shorted by the shunt capacitance, and the Class E behavior has to be clearly approximated. In particular, the voltage wave shaping can be performed recurring to the first harmonic components only (Raab, 2001; Mader et al., 1998), while the ZVS and ZVDS conditions cannot be longer satisfied.

Truncating the ideal voltage Fourier series at the third component, the resulting waveform is reported in Fig. 6, from which it can be noted the existence of negative values. Thus it becomes mandatory to prevent such negative values of drain voltage to respect active device physical constraint and safely operations.

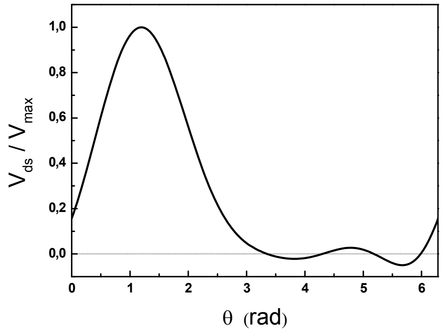
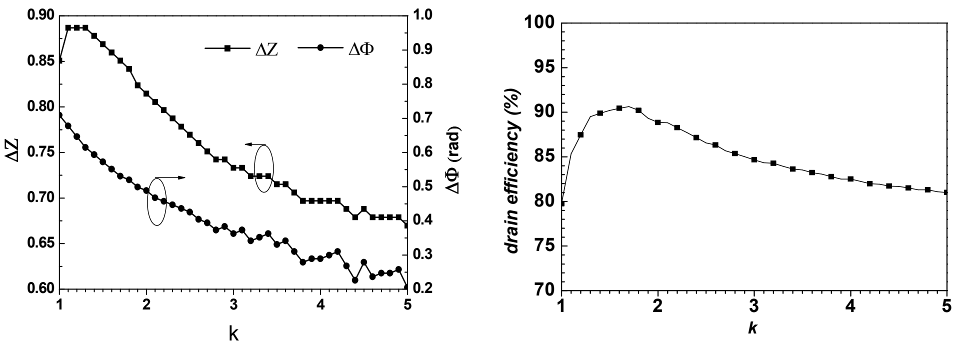


Fig. 6. Three harmonics reconstructed voltage waveform

As pointed out in (Colantonio et al., 2005), two solutions can be adopted. Obviously it is possible to increase drain bias voltage, but it would mean a non negligible increase in the DC dissipated power that in turn causes a decrease in drain efficiency levels. In addition, an increasing on peak voltage value could exceed breakdown limitations of the transistor. The other solution is based on the assumption of unaffected current harmonic components, thus optimizing the voltage fundamental component, while keeping fixed the other harmonics imposed by the network topology (i.e. the filter L_0-C_0 behavior and the device capacitance C_{ds}) (Cipriani et al., 2008). The optimization process must be implemented in a numerical form in order to reduce complexity and computing effort. The main goal is to avoid negative voltage values on drain voltage and, at the same time, maximize output power, hence efficiency. Then, for every value of frequency exceeding the maximum one, the optimum high frequency fundamental impedance, $Z_{1,HF}$, is optimized in magnitude and phase.



(a) (b)

Fig. 7. Class E optimum load impedance (a) and ideal efficiency (b) as a function of k

Obtained results are expressed as normalized to ideal load impedance at maximum frequency given by (27) and depicted in Fig. 7a as a function of normalized frequency $k=f/f_{Max}$, defined as the ratio between the assumed operating frequency f and the maximum

allowed one f_{Max}, defined in (27). The plot shown in Fig. 7a can be considered as a "design chart" for high frequency Class E development, once the maximum frequency is known.
A quasi monotonic decrease of magnitude of fundamental impedance is observed, leading to a reduced voltage fundamental component and a reduced output power. At the same time, the phase decreases tending to almost purely resistive values. The related drain efficiency is reported in Fig. 7b, showing an increasing reduction with respect the ideal 100% value due to non ideal operating conditions.
A high frequency Class E PA example is shown in Fig. 8.

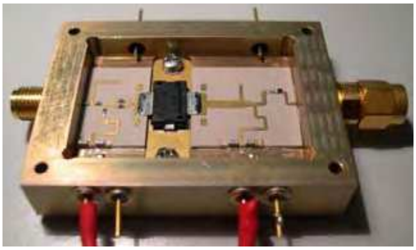


Fig. 8. A 2.14 GHz LDMOS Class E PA

The amplifier is designed using a medium power LDMOS transistor for base station application at 2.14 GHz. Once the bias point, maximum current and output capacitance of the transistor are fixed, the maximum frequency in Class E mode is directly derived. Considering a maximum current of 2.5 A, a bias voltage of 20 V and an output capacitance of 4.2 pF (estimated by S- parameters simulation), the maximum frequency in Class E results in 520 MHz, far below the frequency chosen for the design. If operating at 520 MHz, the load impedance would be $Z_1=25.1e^{j36°}$. At 2.14 GHz (4.1 times above f_{Max}), the load impedance is directly obtained by the design chart of Fig. 7a resulting in $Z_{1,HF}=17.5e^{j17°}$. Since a very simple equivalent model of the device is used, as Fig. 2 shows, this impedance is seen at the nonlinear current source terminals, so that eventual parasitic and package effects should be considered as belonging to the output load.

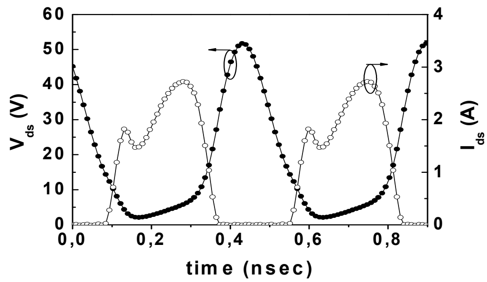


Fig. 9. Simulated voltage and current drain waveform of the designed PA

Simulated drain current and voltage waveform are depicted in Fig. 9, with reference to the internal nodes of the model. A good agreement with typical Class E waveform is remarkable, above the maximum frequency, although the perfect switching behavior cannot be satisfied.

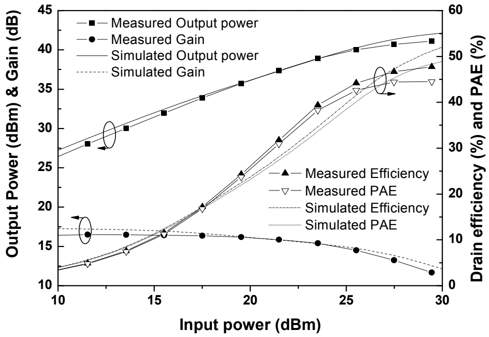


Fig. 10. Simulated and measured output performance of the designed PA

3.4 Class E matching network implementation and other topologies

Although Class E approach has basically a fixed circuit topology, different solution can be adopted for the synthesis of output matching network. Depending on the design frequency, distributed approaches are possible: proper load conditions at fundamental have to be satisfied, according to (24), and an open circuit condition must be provided at harmonics of the fundamental frequency, usually second and third harmonics (Negra et al., 2007; Wilkinson & Everard, 2001; Xu et al., 2006).
In Fig. 11a, no lumped elements are used unless block capacitors, while the 50Ω matching is synthesized through a very compact and simple structure reported in Fig. 11b (Mader et al., 1998). In order to provide harmonic suppression on the load, different quarter-wave open stubs can be used at different harmonics (Negra et al., 2007), while series transmission lines and wave impedances are properly chosen to provide the correct fundamental load.

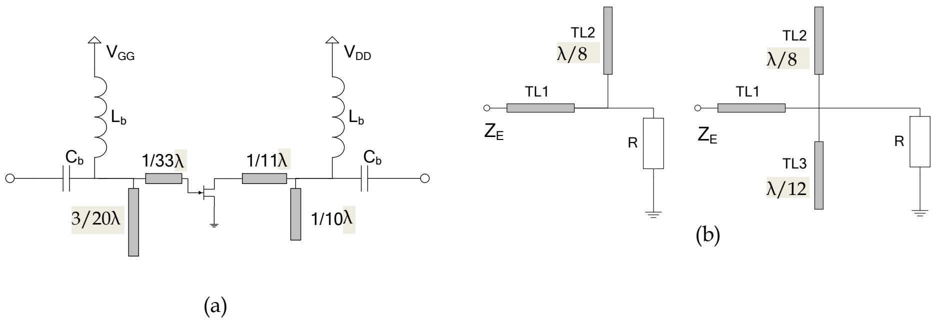


Fig. 11. Some practical examples of Class E transmission lines amplifiers.

Additionally, different circuit topologies exist that can provide the same results as the classical formulation: they have been widely investigated in (Grebennikov, 2003) and are commonly referred as parallel circuit Class E and their main characteristic is the presence of

a finite parallel inductor in the output network, required for the output device biasing supply, as reported in Fig. 12. As before assumed, the shunt capacitance C includes the transistor output capacitance C_{ds}.
The first circuit, in Fig. 12a, employs a very simple output matching network, which consist of a parallel inductor and a series blocking capacitance. Applying ZVS and ZVDS conditions on this circuit, and considering the transistor to behave as a perfect switch, the solution of the circuit is given by a second order non homogeneous differential equation, given by (28), which has to be solved in order to determine the value of all circuit parameters.

$$\omega^2 LC\frac{d^2 v_s(\omega t)}{d(\omega t)^2}+\frac{\omega L}{R}\frac{dv_s(\omega t)}{d(\omega t)}+v_s(\omega t)=V_{DD} \tag{28}$$

The values of reactive components, L and C, are:

$$C=\frac{1.025}{\omega R} \qquad L=0.41\frac{R}{\omega} \tag{29}$$

and the load resistance R is determined using the desired output power at fundamental frequency, P_1:

$$R=1.394\frac{V_{DD}{}^2}{P_1} \tag{30}$$

Due to the lack of any filtering action at the output, this circuit becomes not practical in applications - like telecommunications - which require harmonic suppression (Grebennikov, 2003). Moreover, a higher peak current value is obtained ($4.0 I_{DC}$ instead of $2.862\ I_{DC}$ for the classical topology) that has to be taken into account in the choice of the active device.
The circuit in Fig. 12b adds a series LC filter in the output branch and it is very similar to a canonic Class E amplifier using a finite DC feed inductance, unless for the absence of the “tuning” series inductance. Providing a high Q factor for the LC series filter, the current i_R flowing into the output branch can be assumed as sinusoidal: this hypothesis is used as starting point for a complete time domain analysis which is similar to what reported in paragraph 4.1. Optimum parallel capacitance C and optimum load resistance R are obtained after inferring the phase angle between in-phase and quadrature components of fundamental current:

$$\psi=\arctan\left(\frac{R}{\omega L}-\omega RC\right)=34.244° \tag{31}$$

From which:

$$C=\frac{0.685}{\omega R} \qquad L=0.732\frac{R}{\omega} \tag{32}$$

Output resistance R is derived from desired fundamental output power, P_1:

$$R = 1.365 \frac{V_{DD}^{\ 2}}{P_1} \tag{33}$$

Slightly different voltage and current peak values (Grebennikov, 2003) are obtained with respect to the traditional Class E approach:

$$V_{Max} = 3.647 \cdot V_{DD} \qquad\qquad I_{Max} = 2.647 \cdot I_{DC} \tag{34}$$

In Fig. 12c the parallel inductance is replaced by a short-circuited short length transmission line: this solution is quite popular at microwave frequencies. In order to approximate the Class E optimum impedance at fundamental frequency, the electrical length and the characteristic impedance of the transmission line are determined starting from the optimum fundamental impedance and according to the relation (Grebennikov, 2003):

$$Z_0 \cdot \tan(\theta) = \omega L. \tag{35}$$

The load impedance Z_E seen at device terminals should satisfy the optimum impedance at fundamental frequency, and remembering relation (31) it is rewritten as:

$$Z_E = \frac{R}{1 - j\tan\psi} \tag{36}$$

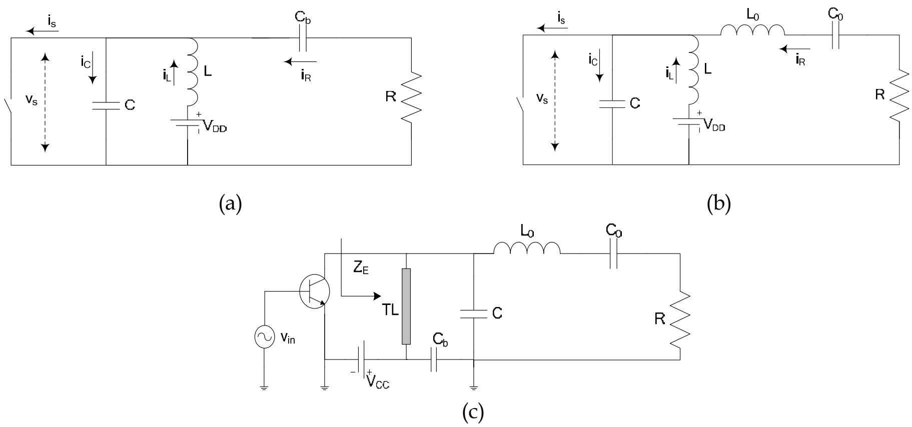


Fig. 12. Parallel circuit Class E topology (a), parallel circuit Class E with output filter (b) and transmission line parallel Class E (c).

Finally, using equation (32) to determine the optimum required parallel inductance, the electrical length of the parallel transmission line can be obtained:

$$\tan\theta = 0.732 \frac{R}{Z_0} \tag{37}$$

4. The inverse Class E amplifier

The Inverse Class E amplifier, or voltage drive Class E amplifier, is commonly considered as the dual version of the Class E amplifier, in which current and voltage waveforms are interchanged, as shown in Fig. 13. It is also referred as "series-L/parallel tuned Class E", being the traditional topology defined as "parallel-C/series-tuned Class E" (Mury & Fusco, 2005; Mury & Fusco, 2007).

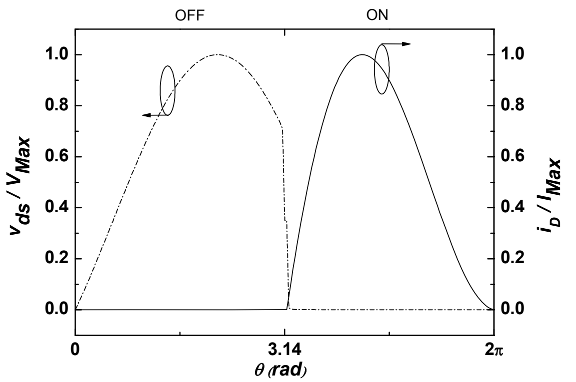


Fig. 13. Ideal inverse Class E waveforms.

A former version of the Inverse Class E amplifier was reported in (Kazimierczuk, 1981): the circuit does not have shunt capacitor, while a series tuned filter and a finite DC feed inductance is considered in the output network, as depicted in Fig. 14. Although this circuit seems to be similar to those reported in Fig. 12, it implies a different behavior, due to the different characteristic of the shunting element (an inductor instead of a capacitor). When the switch is open, and provided a high enough *Q* factor of the series filter, the only current flowing in the circuit is the sinusoidal output current i_R, that is the inductor current i_L. The latter causes a voltage drop across the inductor, v_L, which has a cosinusoidal form. When the switch is closed, the voltage across the inductor is instantaneously constant and equal to V_{DD}. This causes a linear increase in the current i_L. The current across the switch is calculated as the difference between i_L and i_R and assumes the typical asymmetrical shape.

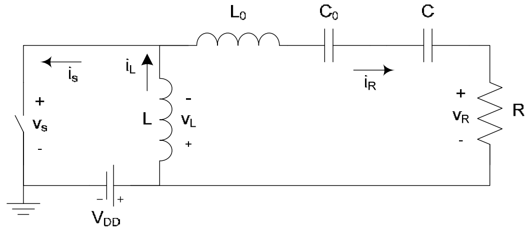


Fig. 14. Inverse Class E amplifier: no-shunt-capacitor/series-tuned topology with finite inductance.

A complete analysis of the inverse Class E amplifier is reported for the first time in (Mury & Fusco, 2005; Mury & Fusco, 2007), together with a defined topology which is shown in Fig. 15 and which is substantially different from the previous version given in (Kazimierczuk, 1981). As can be seen by a comparison of Fig. 15 and the circuit depicted in Fig. 2, each component of the traditional Class E amplifier has been replaced by its dual element in a dual configuration. A DC blocking capacitance C_b is inserted in order to prevent inductance L_0 from shorting the bias voltage.

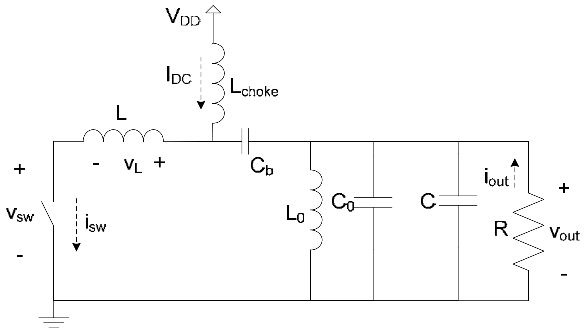


Fig. 15. Inverse Class E amplifier.

Hence, the analysis of the inverse Class E amplifier can be carried out starting from the assumption of a purely sinusoidal output voltage across the output resistance R, which produces a voltage across the inductor L given by:

$$v_L(\theta) = V_{DD} - v_o(\theta) = V_{DD} \cdot \left(1 - a \cdot \sin(\theta + \phi)\right) \tag{38}$$

This is the voltage present across the switch during the OFF time, while during the ON time the switch has no voltage across it and its current is given by integration of (38):

$$i_{SW} = \frac{1}{\omega L} \cdot \int_0^{\theta} v_L(\theta) d\theta \tag{39}$$

These expressions have the same form of those reported in paragraph 4.1, unless current and voltage are interchanged: the same kind of analysis as Class E can be performed on the Inverse Class E circuit. As a consequence, the same numerical results are obtained for the dual configuration, and are summarized in Table 1, referred to a 50% duty cycle operation. As can be seen, the maximum allowable voltage for the Inverse Class E operation is much smaller than for Class E: this is an unquestionable advantage of such a circuit, because the requirement on device breakdown can be drastically relaxed.

However, it is worth to notice that in Inverse Class E amplifier the output capacitance of the active device is not taken into account and set to zero in the ideal analysis: in real world circuit, this is clearly not true. Hence, some actions have to be taken in order to compensate its presence (e.g. a shunt inductance).