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The Progress and Challenges of Applying High-k/Metal-Gated Devices to Advanced CMOS Technologies

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1. Introduction

1.1 Motivation for implementing high dielectric constant gate dielectric for advanced CMOS scaling

Semiconductor devices need to have good performance, with a low cost and low power dissipation. For decades, research and development of semiconductor processing technology and device integration have focused on enhancing performance and reducing costs using SiO_2 as the gate dielectric and doped polysilicon as the gate electrode. The most effective way to enhance performance and reduce costs is to scale the device gate length and gate oxide. Scaling the gate length results in fabricating more devices per wafer (i.e., increase the device density) and thus reduce the cost per chip, while scaling the gate oxide enhances the drive current and reduces the short channel effects due to gate length scaling. However, as the gate oxide becomes thinner, the power to operate transistors increases because of greater gate oxide leakage current. To resolve this high gate oxide leakage problem, the mechanism of the carriers tunneling through the gate dielectric must be better understood. In an ideal metal-insulator-semiconductor (MIS) device, the current conduction in the insulator should be zero. In a real MIS device, however, current can flow through the insulating film by various conduction mechanisms. The two primary conduction mechanisms for electron tunneling through high quality gate dielectric are discussed below.

1.1.1 Direct tunneling

In a metal-insulator-semiconductor (MIS) stack, when the oxide voltage (V_{ox}) is smaller than the metal-insulator barrier height, the electron tunnels directly from the metal electrode into other semiconductor electrode through the insulator. This is known as the direct tunneling process. The equation for direct tunneling current density (current normalized by device area) is proportional to

$$J_{DT} = A \exp (- m^{1/2} V_b^{1/2} T_{ox}) = B \exp (- m^{1/2} V_b^{1/2} K) \quad (1)$$

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where m is the effective mass of the electron, V_b is the barrier height, T_{ox} is the physical thickness of the gate oxide SiO_2, K is the dielectric constant of the insulator, and A and B are pre-exponential factors. From this equation, one can observe that the T_{ox} or K is the dominating factor in controlling the direct tunnel current density. The tunneling current density increases dramatically as the SiO_2 becomes thinner. In general, the gate leakage increases 100 times for every 0.5 nm that the SiO_2 is thinned. The gate leakage density is as high as the 10 E^4 Amp/cm^2 range for SiO_2 as thin as 1.1 nm. The high gate leakage increases standby power consumption according to the following equation:

$$P_{STANDBY} = (I_{subth} + I_{GIDL} + I_g).V_{dd} \quad (2)$$

Where: I_{subth}: subthreshold leakage current
I_{GIDL}: gate-induced drain leakage current
I_g: gate leakage
V_{dd}: supply voltage

On the other hand, Eq. [1] shows that increasing the dielectric constant of an insulator dramatically reduces the direct tunneling current. This is because the gate oxide physical thickness (T_{ox}) and the dielectric constant K of an insulator are correlated by the equivalent oxide thickness (EOT) defined as

$$EOT = (K_{SiO2}/K_{insulator})T_{insulator} \quad (3)$$

where K_{SiO2} and $K_{insulator}$ are the dielectric constant of SiO_2 and the insulator, respectively, and $T_{insulator}$ is the physical thickness of the insulator. Based on this definition, an insulator material with a five times greater dielectric constant than SiO_2 would require a five times greater physical thickness than SiO_2 to keep the same EOT as SiO_2. Therefore the tunneling current for a device using this insulator would be orders of magnitude lower than that using SiO_2 because the tunneling leakage current decays exponentially as the insulator becomes thicker.

1.1.2 Fowler nordheim tunneling

When the oxide voltage (V_{ox}) is greater than the metal/insulator barrier height, the electron tunnels from the metal electrode into the insulator conduction band first and then travels toward the other semiconductor electrode. This is known as the Fowler-Nordheim (FN) tunneling process. The equation for FN tunneling current density is proportional to

$$J_{FN} = C \exp (- m^{1/2} V_b^{3/2} T_{ox}) = D \exp (- m^{1/2} V_b^{3/2} K) \quad (4)$$

where C and D are pre-exponential factors. From this equation, one can observe that the barrier height is the dominating factor in controlling the FN tunnel current density.

Table 1 compares the exponent (the product of m, V_b, and K) shown in the equations of direct tunneling (low field) and FN tunneling (high field) for insulator materials with different V_b and K values. The results show the following:

1. Although oxynitride processed by incorporating nitrogen into SiO_2 was developed to increase the dielectric constant, the reduction of leakage current density is not enough to be used for highly scaled devices such as for the 45 nm technology node. Even for pure nitride (Si_3O_4) shown in the table, the exponent shown in the direct tunneling

equation is only about two times greater than that for SiO_2 while the exponent shown in the FN tunneling equation is similar to that of SiO_2.

2. On the other hand, it is clear that an insulator with a *K* value of 25 reduces the exponent significantly in the direct tunneling Eq. [1] and more than two times in the FN tunneling Eq. [2].

Material	V_b (Volts)	K	Low Field	High Field
SiO_2	3.0	3.9	-6.75	-20.3
Si_3N_4	2.0	7.8	-11.0	-22.1
Ta_2O_6, HfO_2, ZrO_2	1.5	25	-30.6	-45.9

Table 1.

1.2 Motivation for implementing metal gates for advanced CMOS scaling

1.2.1 SiO_2/Polysilicon stack

Figure 1 shows a schematic of a MOSFET in which the gate oxide is SiO_2 and the gate electrode is doped polysilicon. Figure 2 shows the equivalent circuit of an MOS capacitor. The total MOS capacitance C_g can be expressed as

$$C_g^{-1} = C_{ox}^{-1} + C_s^{-1} + C_p^{-1} \quad (5)$$

where C_{ox} is the oxide capacitance, C_s is the silicon capacitance, and C_p is the polysilicon gate electrode depletion capacitance.

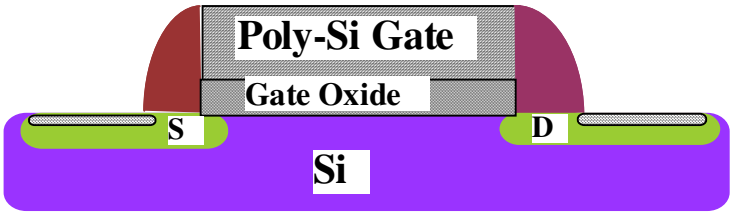

Fig. 1.

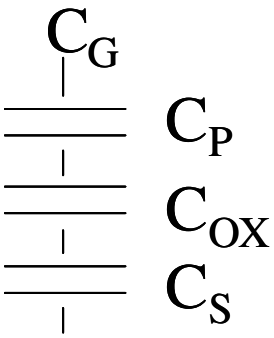

Fig. 2.

When the MOSFET is operated in inversion mode, the doped polysilicon gate energy band bending and charge distribution form a thin space-charge region. This results in a finite, bias-dependant value of C_p and causes polysilicon depletion. The C_p will reduce the value of the C_{ox} for an applied gate voltage (V_g), which, in term, will degrade the MOSFET performance. Although the C_p can be reduced by increasing the dopant concentration in the polysilicon gate electrode, a high dopant concentration would result in dopant penetrating the gate oxide and induce a threshold voltage (V_t) instability problem. On the other hand, using a metal gate as the gate electrode could eliminate the polysilicon gate depletion problem without V_t instability concern because there is no need for dopant to be incorporated into the gate electrode. Another advantage of a metal gate is that the resistance of the metal gate electrode is less than a polysilicon gate.

1.2.2 High dielectric constant insulator compatibility with gate electrode

The compatibility of polysilicon gate electrodes with high dielectric constant (high-k) insulators raises some concern. Most metal oxides with a high dielectric constant used as a gate insulator react with polysilicon and degrade the gate dielectric. Furthermore, this interaction makes it difficult to control the MOSFET threshold voltage. On the other hand, a metal gate is more compatible with high-k metal oxides.

2. Materials screening of high dielectric constant insulators and metal gates

2.1 High-k gate dielectric screening

2.1.1 Issues of high-k gate dielectric

Some fundamental issues with implementing a high-k gate dielectric in MOSFETs are as follows:

- Thermodynamic stability of high-k on silicon
- Trade-off between the dielectric constant (K) and band gap (E_g)
- Film microstructure: crystalline vs. amorphous
- O_2 and dopant diffusion through the grain boundary
- Impact of the amorphous interfacial layer (IL) on the overall dielectric constant of the film, EOT scalability, interfacial roughness, and MOSFET mobility
- Possible mobility degradation and high fixed charge caused by a high-k insulator
- Compatibility with the gate electrode

a. Thermodynamic stability of high-k on silicon
   An analysis of the Gibbs free energies governing the following chemical reactions for metal-Si-oxygen ternary systems is important in predicting stability.
   To avoid instability with Si to form SiO_2,

$$Si + M_{ox} \rightarrow M + SiO_2$$

   To avoid silicide formation,

$$Si + M_{ox} \rightarrow M_{Si} + SiO_2$$

b. Trade-off between the Dielectric Constant (K) and Band Gap (E_g)
   From the direct tunneling Eq. [1], it is desirable to find an insulator with a high dielectric constant and high barrier to ensure low gate leakage current density. Since the barrier height values for most high-k metal oxides are not reported, the closest and most readily available indicator for the band offset is the band gap values. Figure 3 shows the plot of band gap versus dielectric constant for various metal oxides.

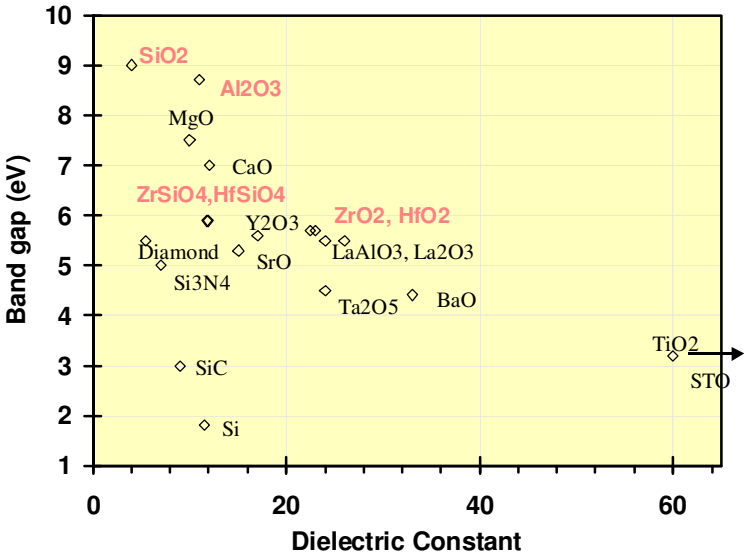

Fig. 3. The trade-off between dielectric constant and band gap limits the choice of metal oxides.

c. Film Microstructure: Crystalline versus Amorphous
For polycrystalline metal oxide, the triple point may generate defects/voids, which will cause a device yield issue. In addition, oxygen, dopant, and impurities diffuse swiftly in the polycrystalline structure primarily through the grain boundary and degrade the electrical properties of the gate stack. Another potential concern is controlling the grain size among small devices and wafers. Amorphous metal oxides can reduce O_2 and dopant diffusion and lower defectivity; however, they usually have a lower dielectric constant than those metal oxides with a polycrystalline structure.

d. Oxygen Diffusion through the Grain Boundary of Metal Oxide
There is a distinct processing difference between the metal oxides and conventional thermal oxide SiO_2. Metal oxides are deposited on the silicon substrate instead of thermally grown like SiO_2. The intrinsic quality of the deposited film is inferior to thermally grown film. A post-deposition anneal under dilute oxygen ambient is necessary for high performance devices. Most metal oxides with a high dielectric constant, however, form a crystalline structure after a relatively high temperature anneal. Therefore the oxygen contained in the ambient of the post-metal oxide deposition anneal diffuses through the grain boundaries of the metal oxides and reacts with silicon substrate, which forms a SiO_2 interfacial layer (IL).

e. Impact of the Amorphous Interfacial Layer (IL) on the Overall Dielectric Constant of the Insulator, EOT Scalability, Interfacial Roughness, and MOSFET Mobility
The SiO_2-like interfacial layer reduces the overall dielectric constant of the bi-layer gate dielectric (high-k on top of a SiO_2 IL). The IL is about 1 nm thick, which would make scaling the EOT to less than 1 nm difficult. The interface between the IL and silicon substrate is rougher than the interface between conventional thermally grown SiO_2 and

silicon, which may degrade channel carrier mobility and generate interface state defects. Figure 4 shows a transmission electron microscopy (TEM) image of the metal oxide MOS structure and the key concerns about the gate stack.

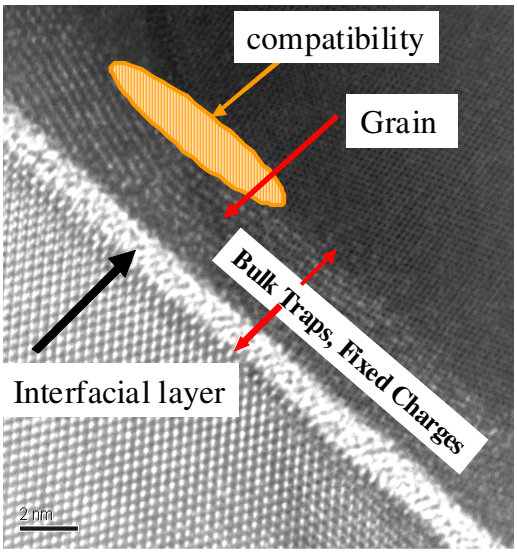

Fig. 4.

f. Possible Mobility Degradation and High Fixed Charge Caused by the High-k Insulator
Soft phonons in the metal oxide bonding structure contribute to the high dielectric constant property of metal oxides. Soft phonons are generated by high atomic number atoms resonating in their bonding structures. These phonons make a lattice contribution to the overall polarizability and therefore the high dielectric constant. There is a concern that the mobility of the channel carriers may be degraded by interactions with these soft phonons.

2.1.2 High-k Gate Dielectric Candidates

a. Metal Oxide
After eliminating the metal oxides that are thermodynamically reactive with silicon substrates or that have a relatively low dielectric constant or small band gap, the remaining candidates fall under group IVB, IIIA, and IIIB of the periodic table.

i. Metal Oxides Used for Memory Capacitors [1, 2, 3, 4]
Candidates such as TiO_2 and Ta_2O_5 have the advantage of having a relatively high dielectric constant and a history of processing in the industry. However, the following concerns make them unattractive for logic devices:

- Small band gap
- Instability with silicon substrates
- High density of oxygen vacancies
- Require an oxygen anneal to improve film quality, which results in oxidation of bottom leading to an undesirable increase in EOT

- Unstable microstructure

ii. Group IIIA and IIIB Metal Oxides: Al_2O_3 and La_2O_3 [5, 6, 7]
Both Al_2O_3 and La_2O_3 are thermodynamically stable with silicon substrates. In addition, Al_2O_3 is amorphous at 1000°C and has a relatively high band gap (8.7 eV ~ SiO_2's value). However, it has a relatively low dielectric constant; high oxygen, B, and P diffusion; and easily absorbs H_2O. La_2O_3 has a relatively high dielectric constant (K ~ 27), but the band gap is small (4.3 eV) and it very easily absorbs moisture from the ambient.

iii. Group IVB Metal Oxides: HfO_2 and ZrO_2 [8-18]
These metal oxides have reasonably high dielectric constants and band gaps (see Figure 3). Both ZrO_2 and HfO_2 devices have demonstrated a many orders of magnitude reduction in gate leakage with an EOT around 1.0 nm and well-behaved transistors. However, they have high O_2 and dopant diffusivity due to their crystalline microstructure. ZrO_2 has a relatively stronger interaction with polysilicon gates than HfO_2. Figure 6 shows the interfacial layer thickness beneath ZrO_2 increases as the post-deposition anneal temperature increases from 550 to 650°C.

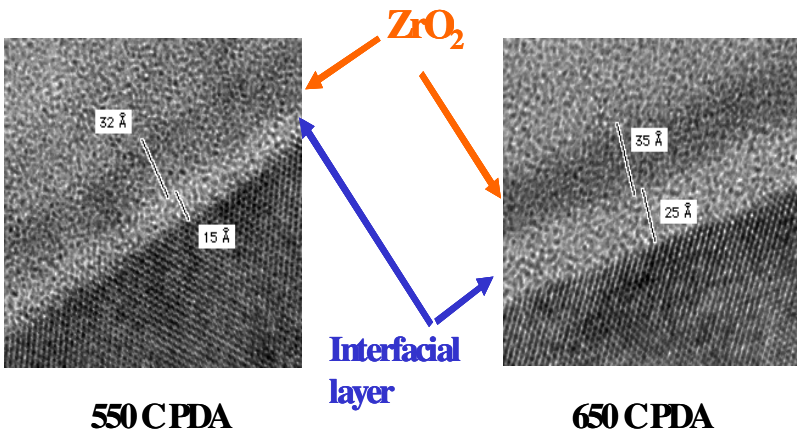

Fig. 6. [13]

Figure 7 shows the x-ray photoelectron spectroscopy (XPS) spectra of the interface between ZrO_2 and the polysilicon gate. The polysilicon gate was deposited in situ on ZrO_2. XPS reveals that ZrO_2 decomposes into a Zr metal compound when the gate stack is annealed in nitrogen at 950°C under ultra-high vacuum leading to a high gate leakage current. It also shows the formation of interfacial SiO_2 between ZrO_2 and the polysilicon gate during polysilicon deposition. These results suggest a strong interaction between ZrO_2 and SiH_4 during polysilicon deposition at 550 to 620°C.

On the other hand, HfO_2 metal oxide is thermodynamically more stable with silicon than ZrO_2. Figure 8 shows the XPS spectra of the interface between HfO_2 and the polysilicon gate. Unlike the ZrO_2 film, the HfO_2 film remains stable after polysilicon deposition and a post-anneal in nitrogen up to 950°C.

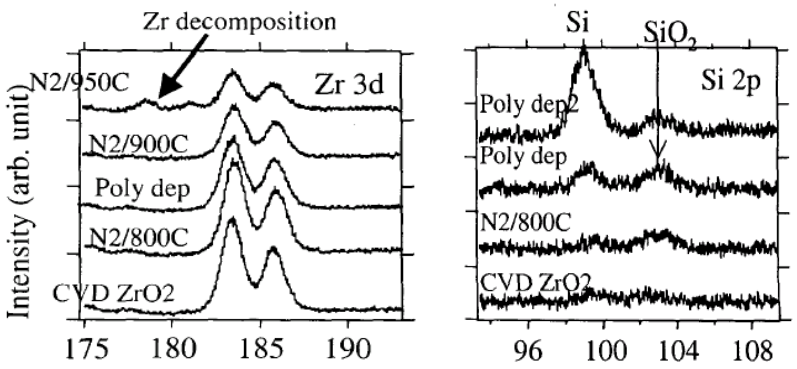

Fig. 7. [14]

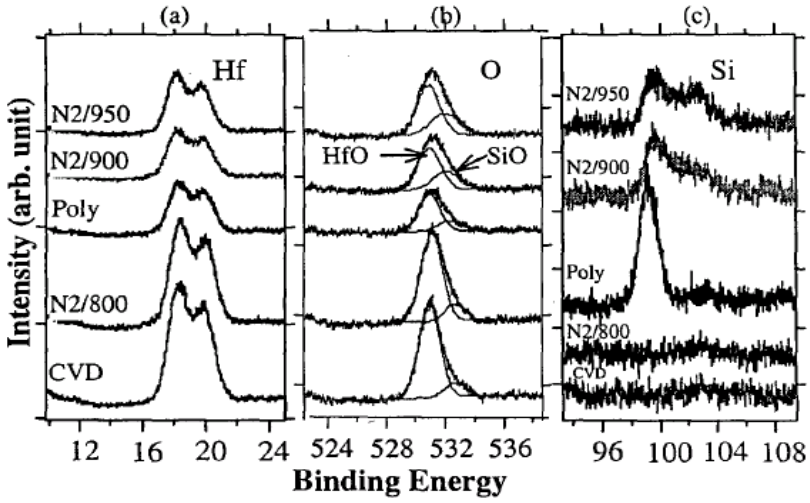

Fig. 8. [9]

b. Metal Silicates (M-Si-O) [19-22]

Adding silicon to metal oxide can maintain the amorphous phase up to a medium temperature such as 800°C depending on the silicon concentration. These metal silicates are thermodynamically stable with the silicon substrate. Figure 9 shows the TEM cross-sections of a gate stack composed of $ZrSi_xO_y$ silicate deposited on a silicon substrate with an aluminum metal electrode. No interfacial layer forms between the zirconium silicate and the silicon substrate after annealing at 800°C for 30 minutes in nitrogen ambient. The interface is atomically sharp, and the film remains amorphous after the anneal. However, there is a possible phase separation with a high temperature anneal and the dielectric constants are lower than metal oxide candidates such as ZrO_2 and HfO_2.

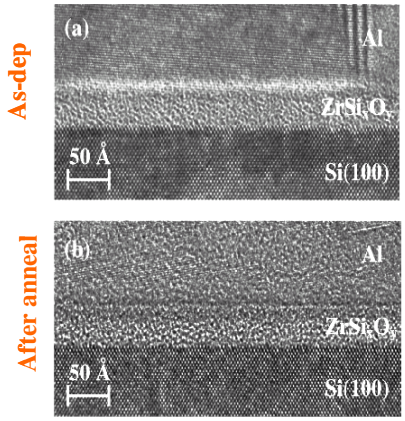

Fig. 9. [21, 22]

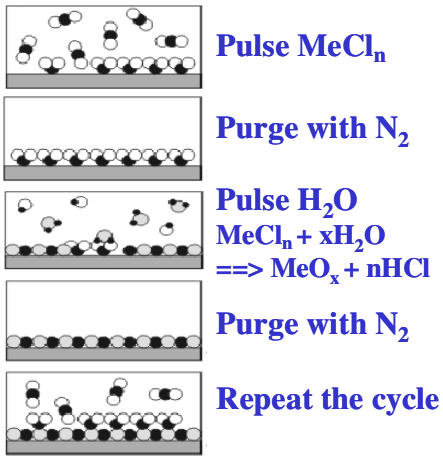

Fig. 10.

2.1.3 High-k dielectric deposition techniques

An important factor in determining the final choice of high-k dielectric is the deposition process, which must be compatible with current CMOS processing, cost, and throughput. In general, there are four major deposition techniques:

- Metal organic chemical vapor deposition (MOCVD) is commonly used, but the C, H, and OH impurities contained in the film are a major concern.
- Physical vapor deposition (PVD) is good for evaluating new materials. However, the purity of the target and plasma-induced damage are common concerns.
- Molecular beam epitaxy (MBE) is good for interfacial control, but the throughput is rather low.
- Atomic layer deposition (ALD) has high uniformity control and good conformality. However, throughput is low and the process is sensitive to surface preparation.

Potential contamination with Cl, C, H, and OH impurities is also a concern. Figure 10 shows a typical ALD process to fabricate metal oxide [23, 24].

In summary, same high-k materials fabricated by different deposition tools, processes, and precursors result in different properties. The final choice of the deposition technique needs to balance cost, throughput, tool reliability, film properties, and device performance and reliability.

2.1.4 High-k gate dielectric device integration issues [17]

a. Device Size Dependence of Gate Current Density

Figure 11 shows that the gate current density of the ZrO_2/polysilicon gate stack has a strong dependence on device size. At 2 V, the leakage current density for the 14 µm NMOS (PMOS) device is 9X (7X) that of a 1.4 µm device. Figure 12 shows the TEM cross-section of the PMOS capacitor with a longer gate length. It is clear that some reactions have occurred at the polysilicon/ZrO_2 interface. The TEM cross-section (Figure 13) shows a nodule extending above and below the polysilicon/ZrO_2 interface. The penetration into ZrO_2 creates a conduction path that results in a high gate leakage current. The longer gate length results in a higher probability that conduction paths will be formed.

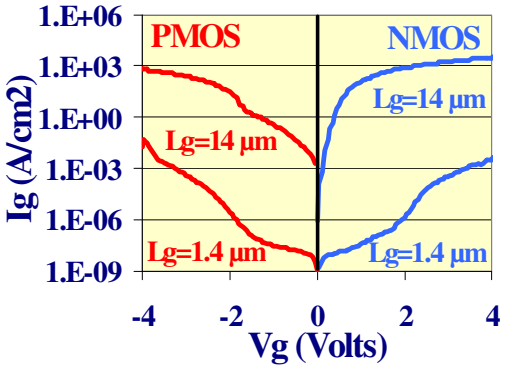

Fig. 11.

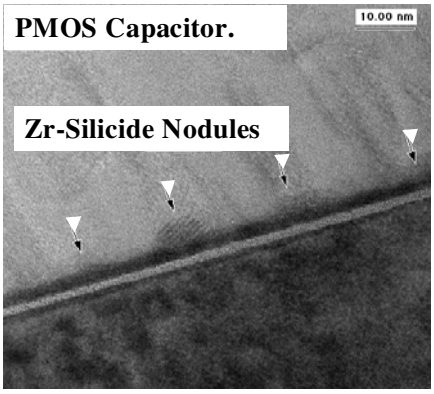

Fig. 12.

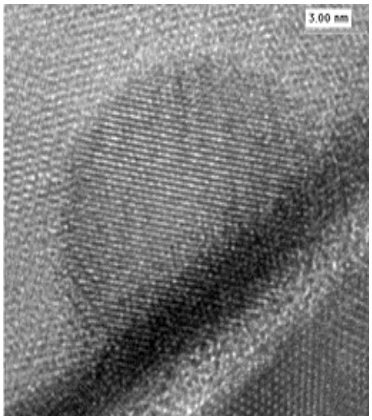

Fig. 13.

b. Lateral Oxidation Model [17]
Figure 14 shows that no nodule is observed at the edge of the devices. A detailed XTEM analysis found the first nodules located ~ 2–3 μm from the edge of the polysilicon gate. This observation suggests that devices with 4–6 μm or smaller gate lengths are nodule-free. It is proposed that active oxygen diffuses through the metal oxide and grows an oxide (SiO_2) at the polysilicon interface (Figure 15). The oxide prevents nodule formation during a high temperature anneal such as a source/drain anneal. Oxidation at the center of large devices is insufficient to prevent the formation of nodules, which cause high leakage current.

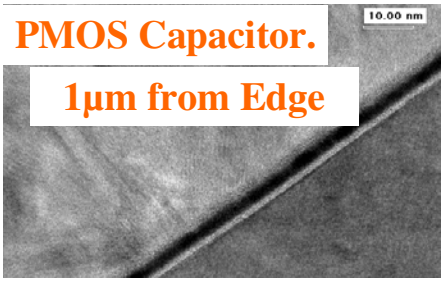

Fig. 14.

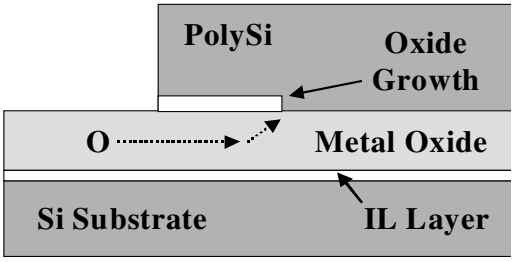

Fig. 15.

2.1.5 High-k dielectric summary

Select high-k metal oxides with thin EOTs have demonstrated an orders of magnitude lower gate leakage than SiO_2. However, it is still a challenge to achieve an EOT thinner than 1.0 nm after transistor fabrication. Degradation in device mobility is observed when using a high-k dielectric. This is more problematic for low EOT applications. Since compatibility with polysilicon gate electrodes is a major concern for some potential metal oxides and metal gate has several advantages, a high-k/metal gate stack is the choice for advanced devices.

2.2 Metal gate electrode materials screening

2.2.1 Materials constraints

A key issue for metal gate materials research is controlling the work function of metal gate electrodes after CMOS processing. There are two choices of metal gate implementation. The first type is a single metal electrode with a work function near the mid-gap (~ 4.6 eV) using additional processing or incorporating additional materials to control the work function of CMOS devices. The second type is a dual metal gate electrode with one metal having a work function (4.1 eV) near the conduction band of the silicon substrate (E_C) for NMOS and the other one having work function (~5.2 eV) near the valence band of the silicon substrate (E_V) for PMOS (Figure 16). The metal electrode materials should have thermal, chemical, and mechanical stability with the high-k gate dielectric and surrounding material during CMOS processing. It is desirable to have a metal gate with a low sheet resistance that is compatible with CMOS process integration, either a conventional "gate first" or replacement "gate last" approach. Metallic elements, compounds (nitrides, silicides, carbides, borides, etc.), and solid solutions are possible candidates.

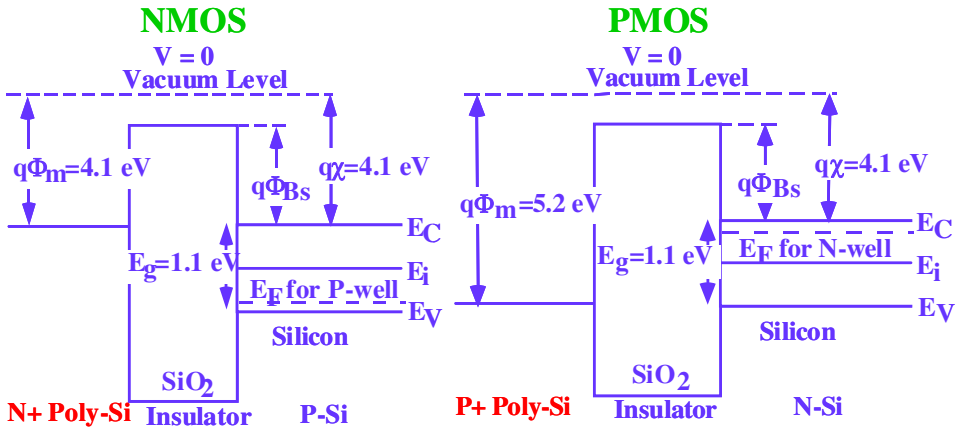

Fig. 16.

Work functions can be obtained from MOSCAPs of various oxide thicknesses using the following equation:

$$V_{fb} = \phi_{MS} + Q_F / C_{OX} \quad (6)$$

An intersect in the Y-axis of the V_{fb} versus EOT plot is the work function (Figure 17). Table 2 shows the work function values for some potential metal gate electrode candidates.

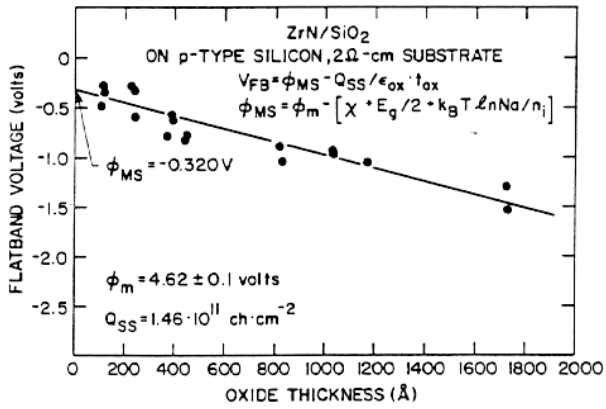

Fig. 17. [25]

Gate Material	Work Function (MOS) (eV)
Ti	4.17, 4.33, 4.6
TiN	4.95
TiSi2	3.67-4.25
Zr	4.05
ZrN	4.6
ZrSi2	-
Ta	4.25, 4.6, 4.15-4.25
TaN	5.41
TaSi2	4.15
Nb	4.3, 4.02-4.3
NbN	-
NbSi2	4.35-4.53
W	4.75, 4.72, 4.55-4.63
WNx	5
WSi2	4.55-4.8
Mo	4.64, 4.53-4.6
MoN	5.33
MoSi2	4.6-4.8, 4.9
Al	4.1

Table 2.

2.2.2 Metal electrode material deposition method and film properties

Metal deposition processing parameters and post-deposition processing affect the metal film properties such as resistivity, microstructure (grain size and orientation), stress, and adhesion. Deposition processes such as CVD and PVD are common methods. In general, CVD films provide better conformality and negligible damage compared to PVD films, but the process may incorporate contaminants. Atomic layer deposition (ALD) shows excellent conformality, but throughput is low. Figures 18 and 19 show the impact of the metal gate deposition process on device performance and gate leakage current, respectively. The device with a SiO_2/PVD TiN metal gate stack results in lower mobility than CVD TiN or polysilicon gated devices. The devices with a SiO_2/PVD TiN gate stack result in a 100X higher gate leakage current than devices fabricated with CVD and ALD.

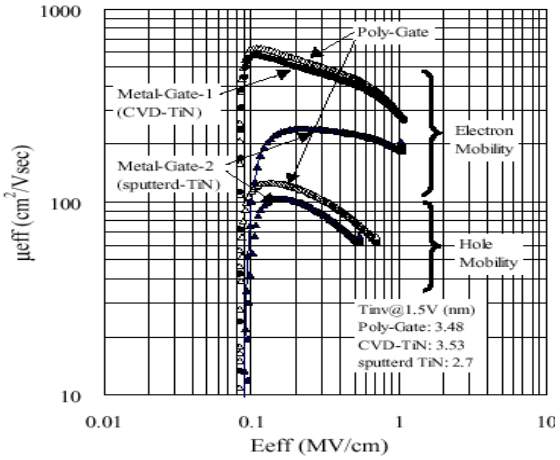

Fig. 18. [26]

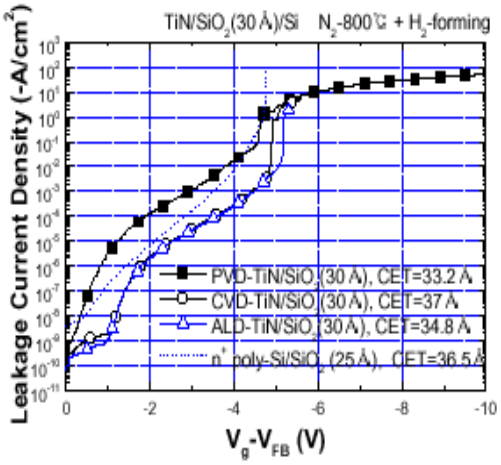

Fig. 19. [27]

2.2.3 Metal gate device integration issues

The dual metal gate approach that needs different metal gate materials for NMOS and PMOS, respectively, increases process complexity dramatically. Contamination (mostly from CVD) and plasma damage (mostly from PVD) affect gate device parameters such as Q_f, D_{it}, V_t stability, and gate oxide integrity. Another concern with metal gates is poor oxidation resistance. The etchability of metal materials, especially selectivity to metal oxides, is a key area for process development.

a. Conventional "Gate First" CMOS Integration
   Conventional gate first integration involves the ability to etch the gate material. For example, Figure 20 shows a nitride/W/TiN gate electrode stack on top of gate oxide. The gate electrode materials must be protected from oxidation or attack by wet chemicals. The gate electrode materials must also be stable with their surrounding materials during high temperature steps. These requirements may limit the choices of materials for metal gate materials along with alternative high-k dielectrics.

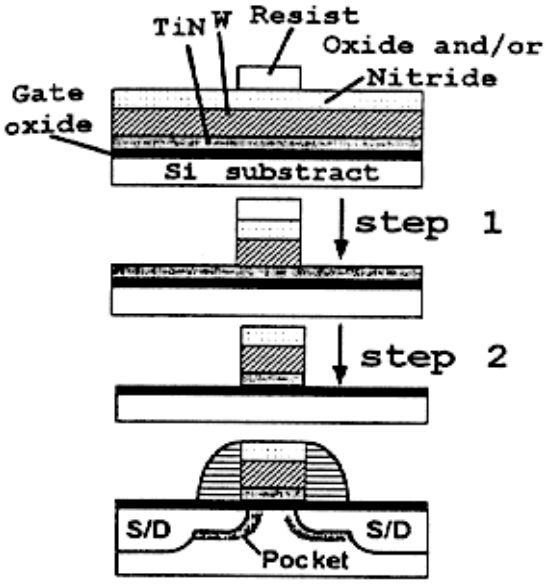

Fig. 20. [28, 29]

b. Replacement "Gate Last" CMOS Integration
   This integration eliminates many constraints posed by conventional "gate first" integration such as process-induced damage, the requirement to etch new materials, thermal/chemical stability concerns, stress-induced diffusion issues. After completing conventional MOSFET fabrication with replacement polysilicon, gate oxide is deposited and using chemical-mechanical polishing (CMP) technique to flatten the top surface (Figure 20a). A wet etch or dry etch process is used to etch off the polysilicon gate (Figure 20b) followed by a new metal gate electrode material and a new gate dielectric deposition (Figure 20c). Another CMP process or a second patterning of the gate is used to form the final structure.

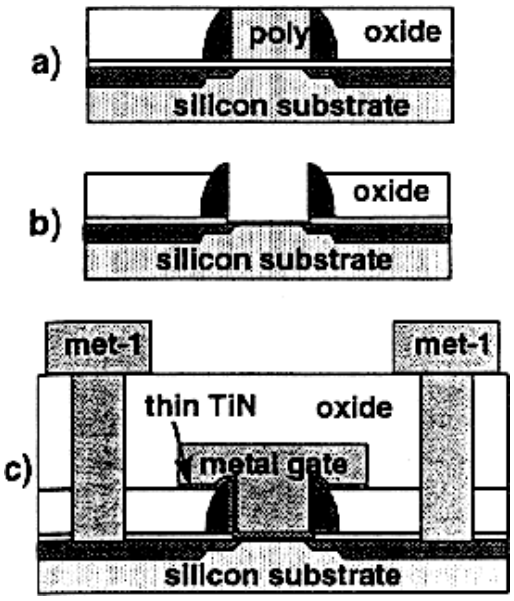

Fig. 20. [30]

c. Summary

A single metal gate with a mid-gap work function may not be able to achieve a low MOSFET threshold voltage and boost performance; however, it has potential for fully depleted silicon-on-insulator (FDSOI) applications. Dual metals with work functions similar to n^+ polysilicon and p^+ polysilicon pose significant integration challenges. Thermodynamic and mechanical stability is an important issue in the choice of metal gate materials. Both the gate first and gate last integration have advantages and disadvantages. The final choice of integration scheme will be decided by performance, yield, and cost.

3. Device characteristics using High-k/Metal Gate (HKMG) stack

3.1 Impact of defects in the HKMG stack on device performance and reliability

As mentioned in section 2.1.1.d, the deposited high-k gate dielectric contains a high defect density in the bulk even after a post-deposition anneal (PDA). The quality of the interface between the silicon substrate and interfacial layer (IL) is not as good as the interface between silicon and conventional thermally grown gate oxide SiO_2. A TEM cross-section of the HKMG gate stack, shown in Figure 21, highlights the different regions of the gate stack. The defects in the bulk of the high-k gate dielectric and at the interface between the silicon substrate and IL have a significant impact on device performance and reliability, such as threshold voltage stability. As discussed in Section 2.1.2.a.iii, the best candidate for a high-k dielectric is Hf-based metal oxide. Therefore the following discussion is based on HfO_2/metal gate stacks.

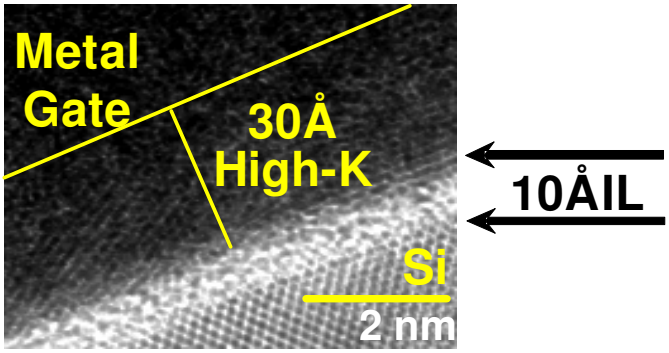

Fig. 21.

3.1.1 Si/IL interface improvement – stressed relaxed pre-oxide [31]

Depositing high-k on top of thick, high quality, thermally grown SiO_2, taking the advantage of its better interface quality, is not desirable because we need a thin gate dielectric to increase transistor speed. To solve this problem, a stress relieved pre-oxide (SRPO) process has been developed to improve the interfacial properties between the high-k dielectric and silicon substrate while maintaining the required thinness to meet the speed enhancement requirement for integrated circuits. The experiment discussed here is as follows. The SRPO is formed by growing a relatively thick thermal oxide with a high temperature anneal (higher than the SiO_2 glass flow temperature of ~ 980°C) for stress relief followed by etching the thermal oxide back to 10 Å using a diluted 700:1 hydrofluoric acid: H_2O solution. The HfO_2 is then deposited by ALD. After the high-k dielectric undergoes a PDA, a TaSiN metal gate is deposited. A commercial CMOS process technology with a source/drain anneal at 1000°C was used to fabricate metal gate/high-k stack nMOSFETs on bulk silicon [32]. Fig. 22 compares the threshold voltage (V_t) shift under constant voltage stress for the control split using the standard process (an RCA clean followed by ALD HfO_2 with a TaSiN metal gate) and the new SRPO process with a TaSiN/HfO_2 gate stack for short channel devices (W/L = 10 μm/0.15 μm). The SRPO with a TaSiN/HfO_2 stack results in a 3X smaller V_t shift than the standard process. These results suggest that devices with the standard process suffer process-induced gate edge damage during transistor fabrication, which increases the V_t shift due to greater trap generation. The process-induced gate edge damage is reduced significantly when using SRPO due to the high quality interfacial layer under the HfO_2, which suppresses interface trap and border trap generation during constant voltage stress. To assess process-induced gate edge damage, the charge pumping current was measured on short channel devices using a pulse string with a fixed base level and varying pulse heights [33] under drain or source bias to detect local charge at the gate edge. The results show less interface and border state trap density for HfO_2/SRPO devices than for HfO_2/RCA devices. The stressed charge pumping results clearly show that the SRPO pre-treatment is much more robust than the RCA pre-treatment under process-induced local charge generation near gate edges. Fig. 23 shows that the normalized transconductance (G_m) of TaSiN-gated short channel devices with SRPO is higher than the standard pre-treatment due to better interface properties with the SRPO process. The fundamental difference between a chemical